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1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.

2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.

3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV

ECN

DESCRIPTION OF REVISION

CK APPD

DATE

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Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-9277	1	SCHEM,MLB,J13	SCH	CRITICAL	
820-3209	1	PCBF,MLB,J13	PCB	CRITICAL	

DRAWING

TITLE=MLB

ABBREV=DRAWING

LAST\_MODIFIED=Thu Feb 23 17:52:06 2012

SCHEM,MLB,J13

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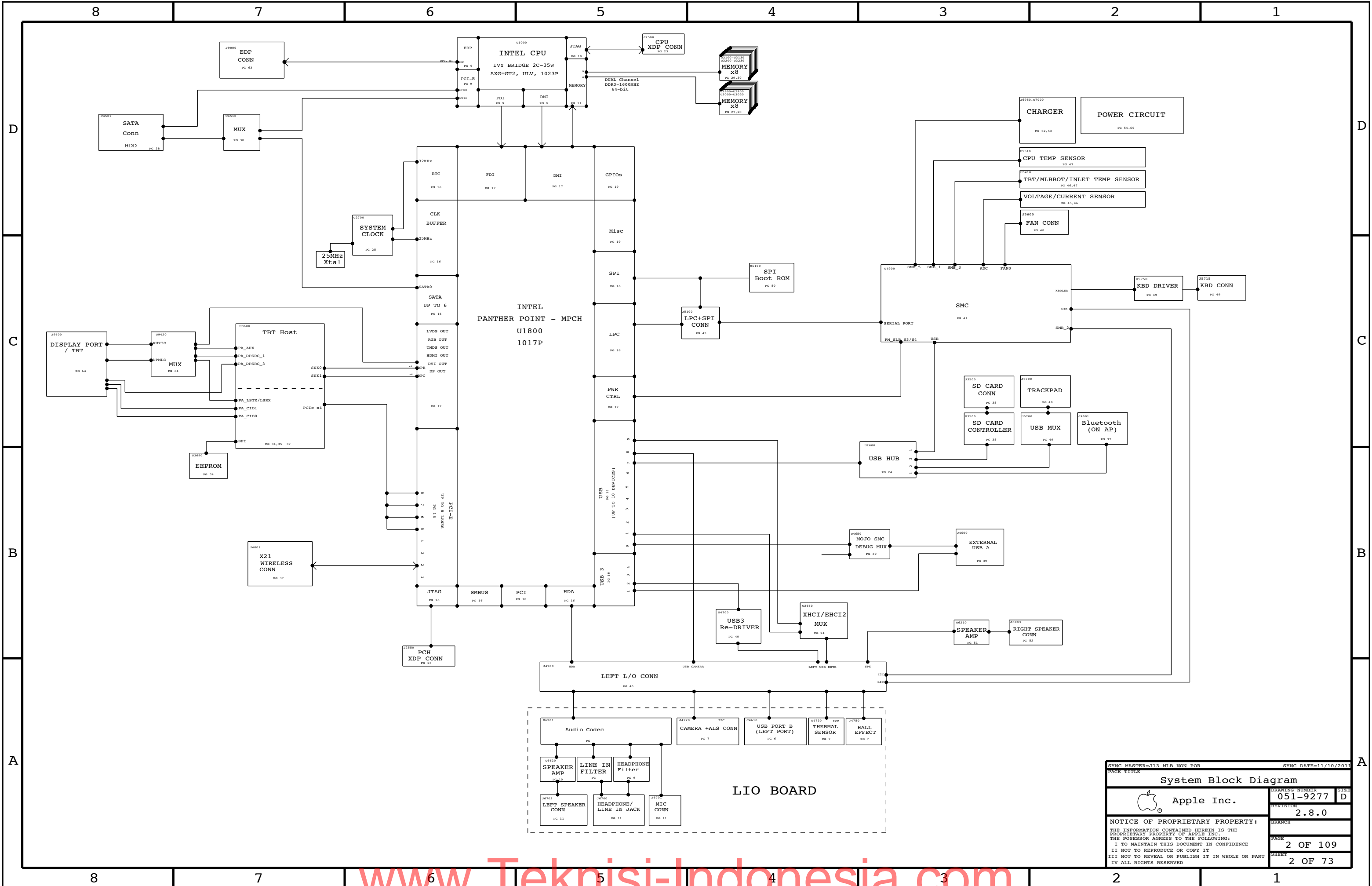
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**J13 POWER SYSTEM ARCHITECTURE**

The diagram illustrates the power system architecture, showing the flow of power from the AC adapter through various regulators, fuses, and sensors to the system components. Key components include the SMC (Super Micro Computer) U4900, COUGAR-POINT (PCH) U1800, and various power management ICs like the ISL6259HRTZ, ISL95870, and TPS22924. The diagram is organized into sections labeled A through D, with a revision history table at the bottom right.

**Revision History**

REV	DESCRIPTION
1	Initial Release
2	Added SMC Power Management
3	Added COUGAR-POINT PCH
4	Added CPU Power Management
5	Added SMC Power Management
6	Added COUGAR-POINT PCH
7	Added CPU Power Management
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95	Added SMC Power Management
96	Added COUGAR-POINT PCH
97	Added CPU Power Management
98	Added SMC Power Management
99	Added COUGAR-POINT PCH
100	Added CPU Power Management

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## J13 BOM GROUPS

BOM GROUP	BOM OPTIONS
J13_COMMON	ALTERNATE_COMMON,J13_MISC,J13_DEBUG:ENG,J13_PROGPARTS,USBHUB2514B,EDP1:YES,PCH_C1
J13_MISC	CPONDR_ELG:NO,HUB_300BREM,TBT:M0:YES,PVS_V5_DCIN:NO,TPAD_PCH:NO,SKIP_S3V3V3:INAUDIBLE,BTWPW:84,TWTV:P15V,LVDOR3_BW:YES,X20_ACOUSTIC:NO
J13_PROGPARTS	BOOTFROM_PROG,SMC_PROG,TBTFROM:PROG
J13_DEVEL:ENG	ALTERNATE,BKLT:ENG,X2P_CONN,X2P_CPU:8PM,X2P_PCH,LCPLUS,DDRREF_DAC,VREFQ:M1_M3,VREFCA:LDO_DAC,60P000_1EL,S3_E0_LED,VCCIOINS_ENG,AIRPORTINS_ENG,HDIOINS_ENG,LCDBKLTIINS_ENG
J13_DEVEL:PVT	LCPLUS,X2P_CONN
J13_DEBUG:ENG	DEVEL_BOM,M0JO:YES,X2P
J13_DEBUG:PVT	DEVEL_BOM,BKLT:PROG,M0JO:YES,X2P,X2P_CPU:8PM,VREFQ:LDO,VREFCA:LDO,VCCIOINS_PROG,AIRPORTINS_PROG,HDIOINS_PROG,LCDBKLTIINS_PROG
J13_DEBUG:ENG	BKLT:PROG,M0JO:YES,X2P,X2P_CPU:8PM,VREFQ:LDO,VREFCA:LDO,LCPLUS,VCCIOINS_PROG,AIRPORTINS_PROG,HDIOINS_PROG,LCDBKLTIINS_PROG
DDR3:HYNIX_4GB	RAMCFG0:I, RAMCFG1:I, RAMCFG2:I, RAMCFG3:I, DRAM_TYPE:HYNIX_4GB
DDR3:HYNIX_8GB	RAMCFG0:I, RAMCFG1:I, RAMCFG2:H, RAMCFG3:I, DRAM_TYPE:HYNIX_8GB
DDR3:SAMSUNG_4GB	RAMCFG0:I, RAMCFG1:H, RAMCFG2:I, RAMCFG3:I, DRAM_TYPE:SAMSUNG_4GB
DDR3:SAMSUNG_8GB	RAMCFG0:I, RAMCFG1:H, RAMCFG2:H, RAMCFG3:I, DRAM_TYPE:SAMSUNG_8GB
DDR3:ELPIDA_8GB	RAMCFG0:H, RAMCFG1:H, RAMCFG2:H, RAMCFG3:I, DRAM_TYPE:ELPIDA_8GB
DDR3:ELPIDA_4GB	RAMCFG0:H, RAMCFG1:H, RAMCFG2:I, RAMCFG3:I, DRAM_TYPE:ELPIDA_4GB

## Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S0865	1	1C,SERIAL SPI KEYPROM,256KBIT,20MHZ,MCP8	U3690	CRITICAL	TBTR0M/BLANK
341S3475	1	1C,EEPROM,CR,V24.1..J11/J13	U3690	CRITICAL	TBTR0M/PROG
338S1098	1	1C,SMC12-A3,40MHZ/50MDIPS MCU,9X9,157BGA	U4900	CRITICAL	SMC_BLANK
338S1065	1	1C,SMC12.40MHZ/50MDIPS MCU, 9X9,157BGA	U4900	CRITICAL	SMC_BLANK
341S3433	1	1C,SMC_V2.1A43,Proto18,J13	U4900	CRITICAL	SMC_PROG
335S0809	1	64 MBIT SPI SERIAL DUAL I/O FLASH_Memory16	U6100	CRITICAL	BOOTROM_BLANK
335S0803	1	64 MBIT SPI SERIAL DUAL I/O FLASH_Memory16	U6100	CRITICAL	BOOTROM_BLANK
341S3482	1	1C,EPI ROM,PROTO18,J13 J11	U6100	CRITICAL	BOOTROM_PROG

## Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
37680855	37680613		ALL	Diodes alt to Toshiba
37680977	37680859		ALL	Diodes alt to Toshiba
37680972	37680612		ALL	Kohm alt to Toshiba
13880676	13880691		ALL	Murata alt to Samsung
37180709	37180652		ALL	KEP alt to KEP
13880671	13880673		ALL	Taiyo alt to Murata
37680790	37680928		ALL	TI alt to Fairchild
15281462	15281295		ALL	Toko alt for MEC inductor
15281085	15281307		ALL	Toko alt for Cyntec
13880703	13880648		ALL	Murata alt to Taiyo Yuden
13880684	13880660		ALL	Murata alt to Taiyo Yuden
15281493	15281300		ALL	Colicraft alt to Murata

35383238	35381428		ALL	Intersil alt to OPA2333
37280186	37280185		ALL	NEF alt to Diodes
37681053	37680604		ALL	Diodes alt to Fairchild
37680855	37680613		ALL	Diodes alt to Toshiba
37680903	37680796		ALL	Fairchild alt to Siliconix
19780431	19780432		ALL	Epson alt to NDK
33784198	33784197		ALL	TDP 1.5GHE alt to Nominal
33784236	33784196		ALL	TDP 1.7GHE alt to Nominal
37180713	37180558		ALL	Diodes alt to ST Micro
12880333	998-4435		ALL	Sanyo alt to Kemet
12880357	998-4435		ALL	Sanyo alt to POS caps
998-4715	998-4435		ALL	Kemet_Bect alt to POS caps
998-4716	998-4435		ALL	Kemet_0045 Plute alt to POS caps

## DRAM CFG CHART

	VENDOR	CFG 1	CFG 0
	HYNIX	0	0
	SAMSUNG	1	0
	MICRON	0	1
	ELPIDA	1	1

SIZE	CFG 2
4GB	0
8GB	1

DIE REV	CFG 3
A	0
B	1

## Module Parts


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4197	1	IVB,QMPS,ES2,K0,1.5,17W,2+2,0.95,4M,ULVB	U1000	CRITICAL	CPU:1.5GHZ
337S4299	1	IVB,QC55,QS,L0,1.7,17W,2+2,1.0,3M,ULVBGA	U1000	CRITICAL	CPU:1.7GHZ
337S4298	1	IVB,QC54,QS,L0,1.8,17W,2+2,1.1,3M,ULVBGA	U1000	CRITICAL	CPU:1.8GHZ
337S4296	1	IVB,QC52,QS,L0,2.0,17W,2+2,1.1,4M,ULVBGA	U1000	CRITICAL	CPU:2.0GHZ
337S4198	1	IVB,QMPS,ES2,K0,1.5,17W,2+2,0.95,4M,ULVB	U1000	CRITICAL	CPU:1.5GHZTDP
337S4236	1	IVB,QMPS,ES2,K0,1.7,17W,2+2,1.0,4M,ULVB,TDP	U1000	CRITICAL	CPU:1.7GHZTDP
337S4165	1	IC,PCH,PPT-MB,SFF,ES1	U1800	CRITICAL	PCH_ES1
337S4180	1	IC,PCH,PPT-MB,SFF,ES2,B0	U1800	CRITICAL	PCH_ES2
337S4235	1	IC,PCH,PPT-MB,SFF,P-QS,C0	U1800	CRITICAL	PCH_C0
337S4275	1	IC,PCH,PPT-MB,Q877,C1,QS	U1800	CRITICAL	PCH_C1
338S1047	1	IC,TBT,CR-4C,ES1,288 PCBGA,12X12MM	U3600	CRITICAL	TBT

333S0622	4	IC, SDRAM, 2GBIT, 256MX8, DDR3-1600, 78P FPGA	U2900, U2910, U2920, U2930	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0622	4	IC, SDRAM, 2GBIT, 256MX8, DDR3-1600, 78P FPGA	U3000, U3010, U3020, U3030	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0622	4	IC, SDRAM, 2GBIT, 256MX8, DDR3-1600, 78P FGBA	U3100, U3110, U3120, U3130	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0622	4	IC, SDRAM, 2GBIT, 256MX8, DDR3-1600, 78P FPGA	U3200, U3210, U3220, U3230	CRITICAL	DRAM_TYPE:HYNIX_4GB
333S0625	4	IC, SDRAM, 4GBIT, 512MX8, DDR3-1600, 82 FPGA	U2900, U2910, U2920, U2930	CRITICAL	DRAM_TYPE:HYNIX_8GB
333S0625	4	IC, SDRAM, 4GBIT, 512MX8, DDR3-1600, 82 FPGA	U3000, U3010, U3020, U3030	CRITICAL	DRAM_TYPE:HYNIX_8GB
333S0625	4	IC, SDRAM, 4GBIT, 512MX8, DDR3-1600, 82 FGBA	U3100, U3110, U3120, U3130	CRITICAL	DRAM_TYPE:HYNIX_8GB
333S0625	4	IC, SDRAM, 4GBIT, 512MX8, DDR3-1600, 82 FPGA	U3200, U3210, U3220, U3230	CRITICAL	DRAM_TYPE:HYNIX_8GB
333S0623	4	IC, SDRAM, 2GBIT, DDR3-1600, 78P FPGA, D-DIE	U2900, U2910, U2920, U2930	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0623	4	IC, SDRAM, 2GBIT, DDR3-1600, 78P FPGA, D-DIE	U3000, U3010, U3020, U3030	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0623	4	IC, SDRAM, 2GBIT, DDR3-1600, 78P FGBA, D-DIE	U3100, U3110, U3120, U3130	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0623	4	IC, SDRAM, 2GBIT, DDR3-1600, 78P FPGA, D-DIE	U3200, U3210, U3220, U3230	CRITICAL	DRAM_TYPE:SAMSUNG_4GB
333S0642	4	IC, SDRAM, 4GBIT, DDR3-1600, 78P FPGA, C-DIE	U2900, U2910, U2920, U2930	CRITICAL	DRAM_TYPE:SAMSUNG_8GB
333S0642	4	IC, SDRAM, 4GBIT, DDR3-1600, 78P FPGA, C-DIE	U3000, U3010, U3020, U3030	CRITICAL	DRAM_TYPE:SAMSUNG_8GB
333S0642	4	IC, SDRAM, 4GBIT, DDR3-1600, 78P FGBA, C-DIE	U3100, U3110, U3120, U3130	CRITICAL	DRAM_TYPE:SAMSUNG_8GB
333S0642	4	IC, SDRAM, 4GBIT, DDR3-1600, 78P FGBA, C-DIE	U3200, U3210, U3220, U3230	CRITICAL	DRAM_TYPE:SAMSUNG_8GB
333S0629	4	IC, SDRAM, 4GBIT, DDR3L-1600, REV B, 78P FPGA	U2900, U2910, U2920, U2930	CRITICAL	DRAM_TYPE:ELPIDA_8GB
333S0629	4	IC, SDRAM, 4GBIT, DDR3L-1600, REV B, 78P FGBA	U3000, U3010, U3020, U3030	CRITICAL	DRAM_TYPE:ELPIDA_8GB
333S0629	4	IC, SDRAM, 4GBIT, DDR3L-1600, REV B, 78P FGBA	U3100, U3110, U3120, U3130	CRITICAL	DRAM_TYPE:ELPIDA_8GB
333S0629	4	IC, SDRAM, 4GBIT, DDR3L-1600, REV B, 78P FGBA	U3200, U3210, U3220, U3230	CRITICAL	DRAM_TYPE:ELPIDA_8GB
333S0628	4	IC, SDRAM, 2GBIT, DDR3L-1600, REV D, 78P FPGA	U2900, U2910, U2920, U2930	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0628	4	IC, SDRAM, 2GBIT, DDR3L-1600, REV D, 78P FGBA	U3000, U3010, U3020, U3030	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0628	4	IC, SDRAM, 2GBIT, DDR3L-1600, REV D, 78P FGBA	U3100, U3110, U3120, U3130	CRITICAL	DRAM_TYPE:ELPIDA_4GB
333S0628	4	IC, SDRAM, 2GBIT, DDR3L-1600, REV D, 78P FGBA	U3200, U3210, U3220, U3230	CRITICAL	DRAM_TYPE:ELPIDA_4GB

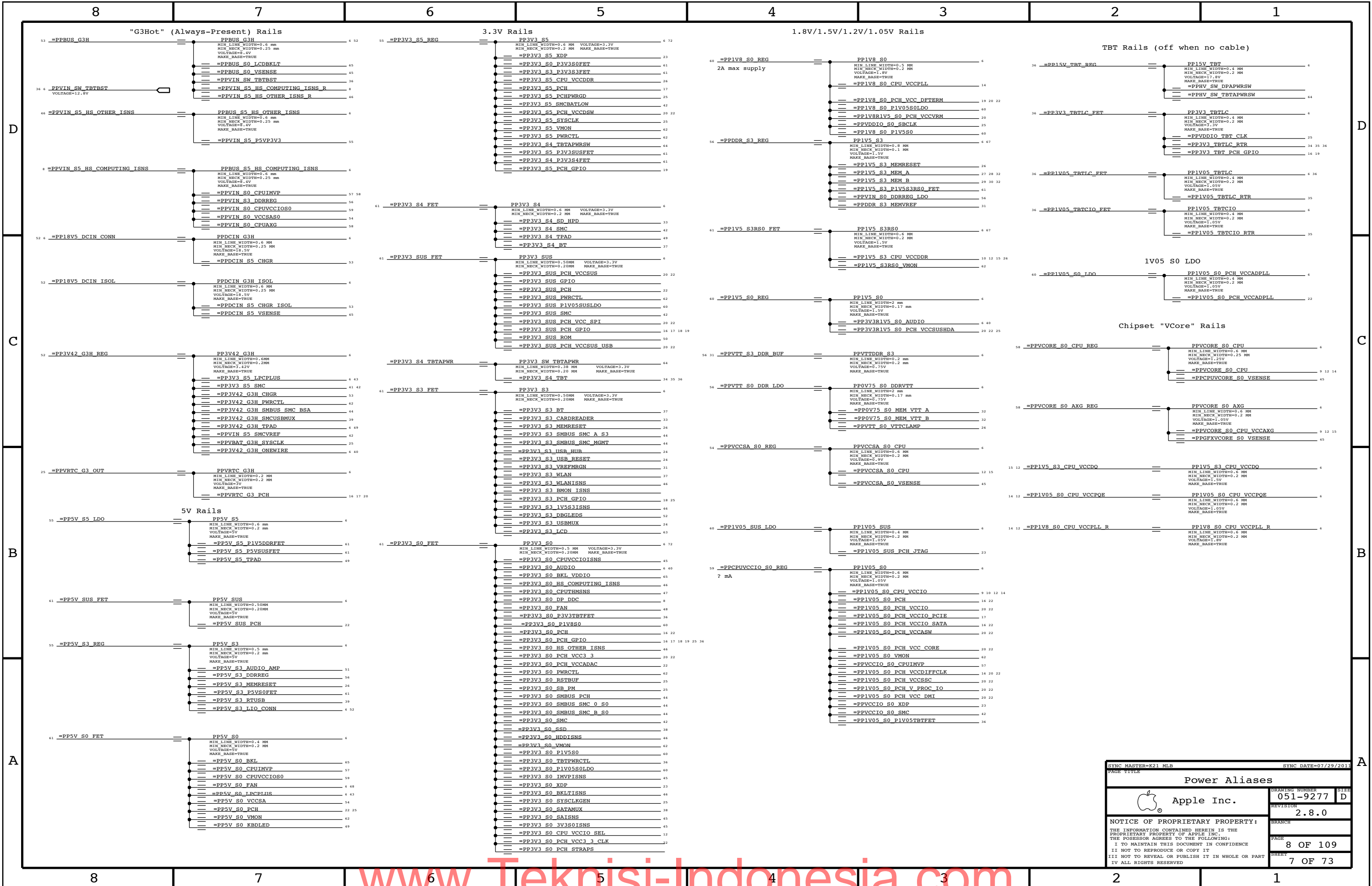
35382929	1	1C,1SL6259,BATCHARGER,3%,4X4MM,QFN28	U7000	CRITICAL
946-3115	1	MLB,DYNAX UV EB 0.220GRAM,K21	GLUE	CRITICAL

## PD Module Parts

806-3142	1	CAN,T29,J11/J13	TBTFENCE	CRITICAL	
806-3215	1	CAN_COVER,T29,J11/J13	TBTCOVER	CRITICAL	
806-3214	1	CAN_TOPSIDE,J11/J13	TBTTOPSIDE_1P	CRITICAL	
806-3706	1	CAN_TOPSIDE_2Pace_Cover,J11/J13	TBTTOPSIDE_2P_COVER	CRITICAL	
806-3705	1	CAN_TOPSIDE_2Pace_Fence,J11/J13	TBTTOPSIDE_2P_FENCE	CRITICAL	
806-3216	1	CAN,MDF,J11/J13	MDPCAN	CRITICAL	
806-3083	1	SHLD,USB_MLB,J11/J13	USBCAN	CRITICAL	
806-2377	1	K78, MDF Spring	MDPSRING	CRITICAL	NOSTUFF

SYNC MASTER=J30 MLB		SYNC DATE=07/27/2011	
PAGE TITLE		PAGE	
BOM Configuration			
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		5 OF 73	

8	7	6	5	4	3	2	1
Functional Test Points							
J4001: AirPort / BT Connector		J5600: Fan Connector		J4501: SATA SSD Connector		J4001: AirPort / BT Connector	
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SYNC DATE=07/29/2013

PAGE TITLE

Power Aliases

 Apple Inc.

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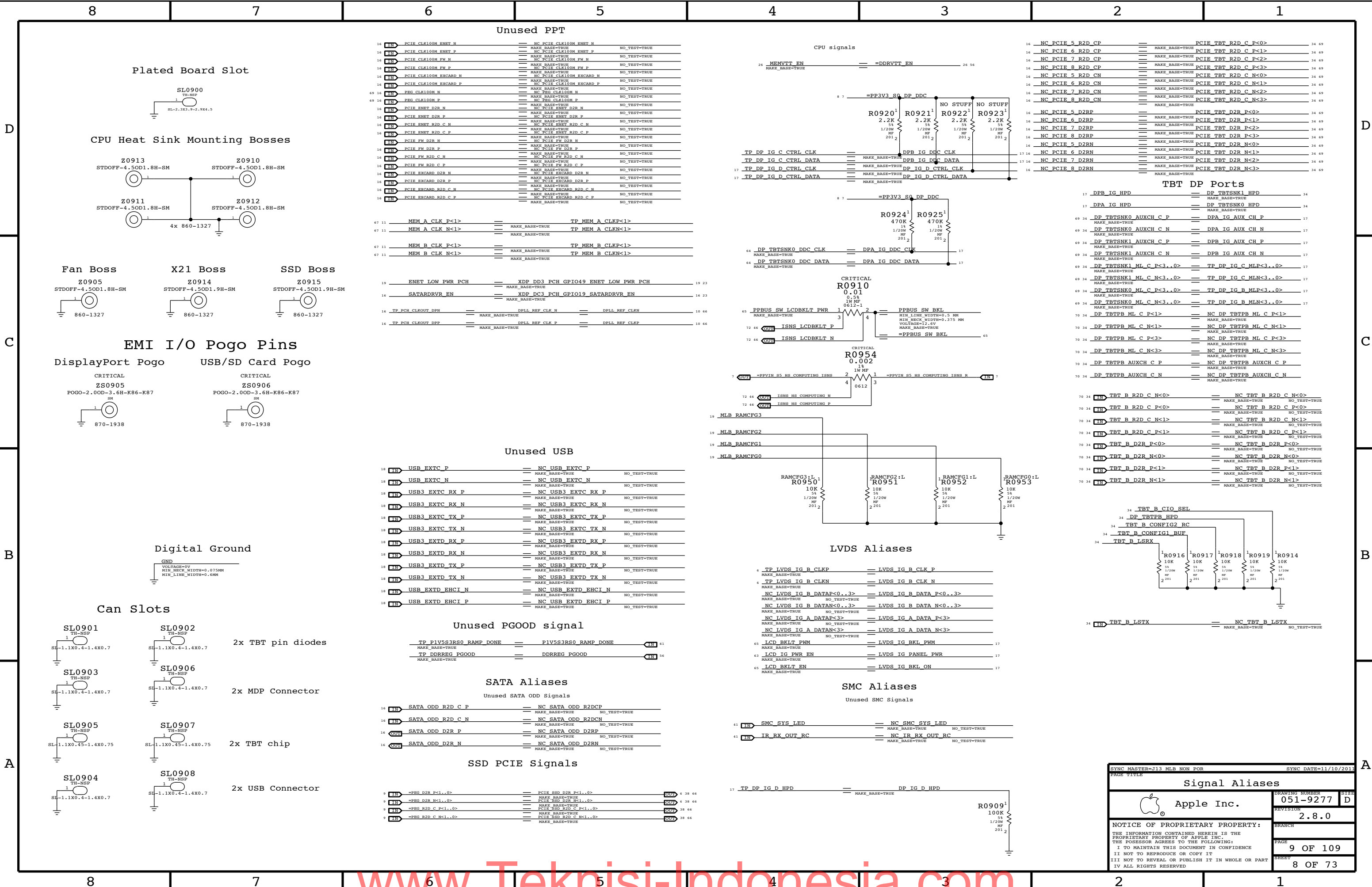
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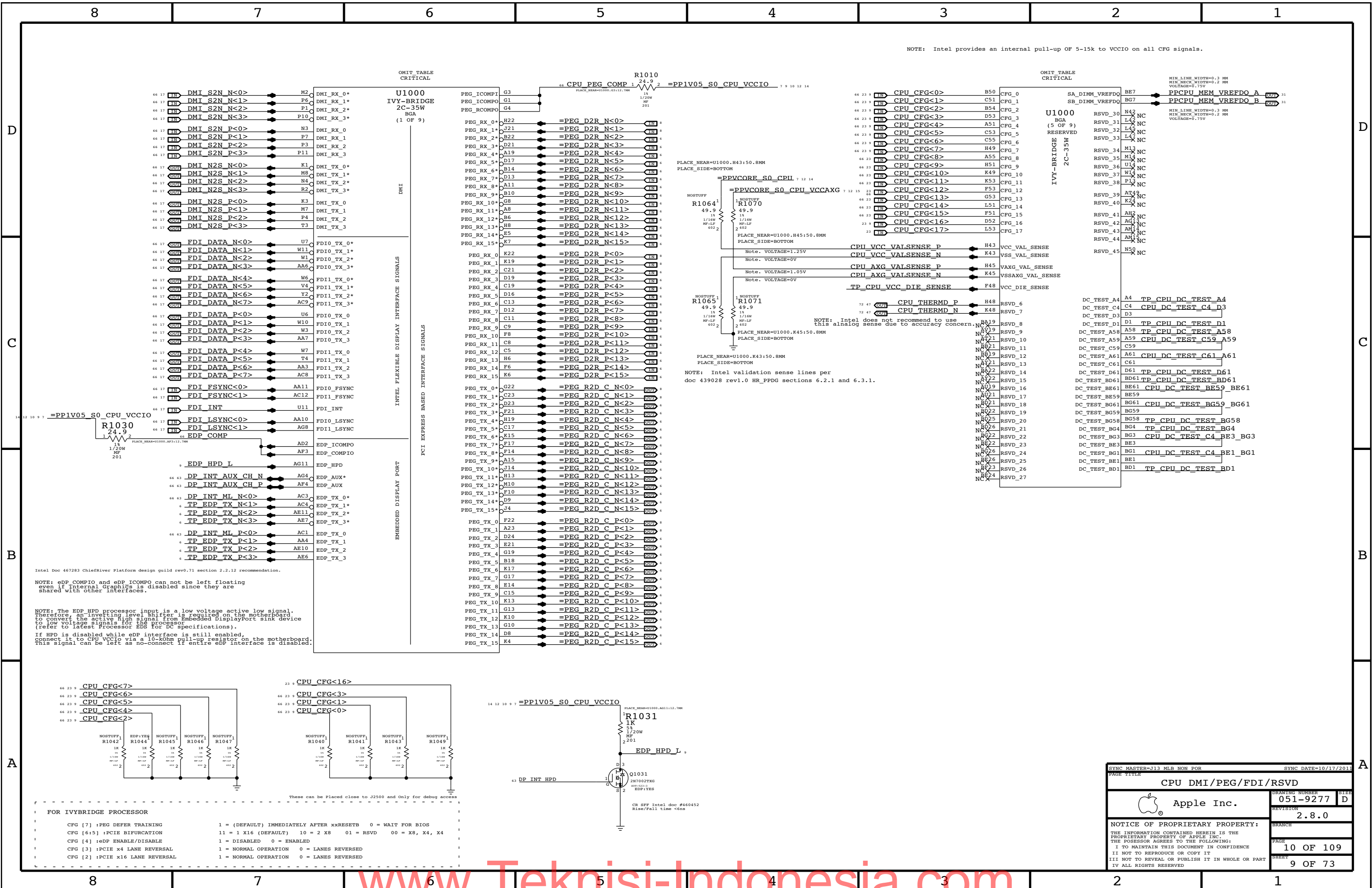
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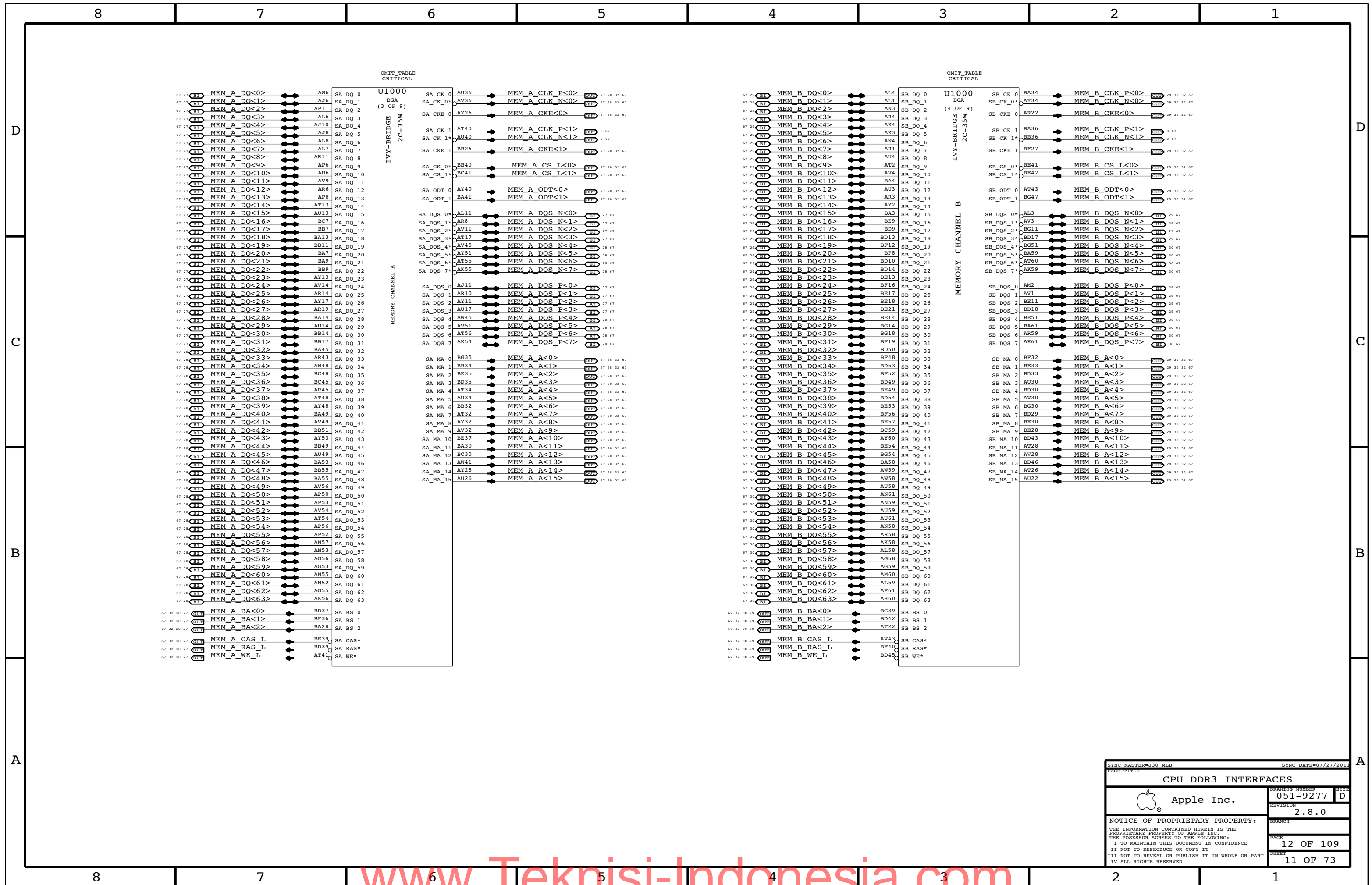
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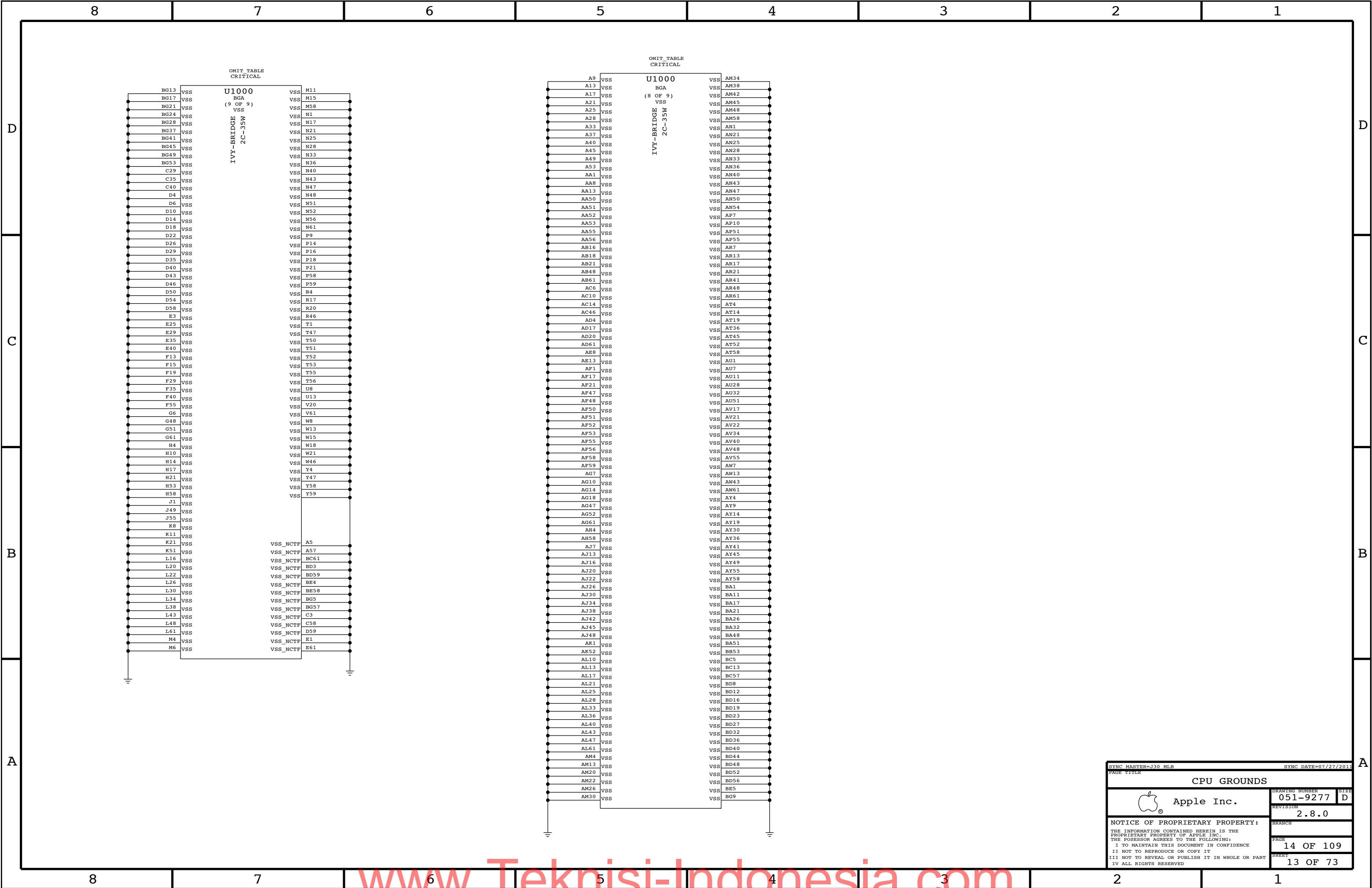


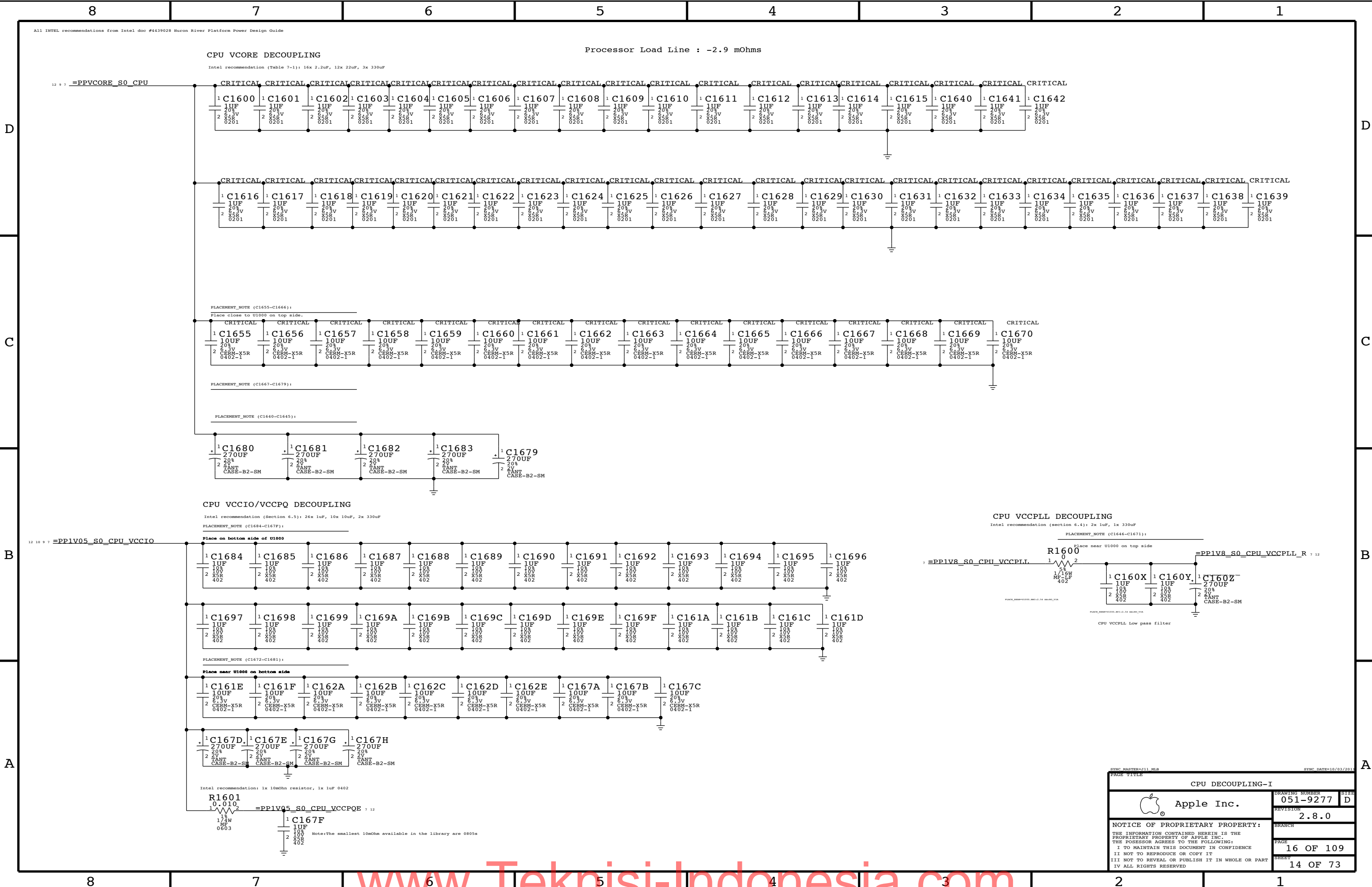




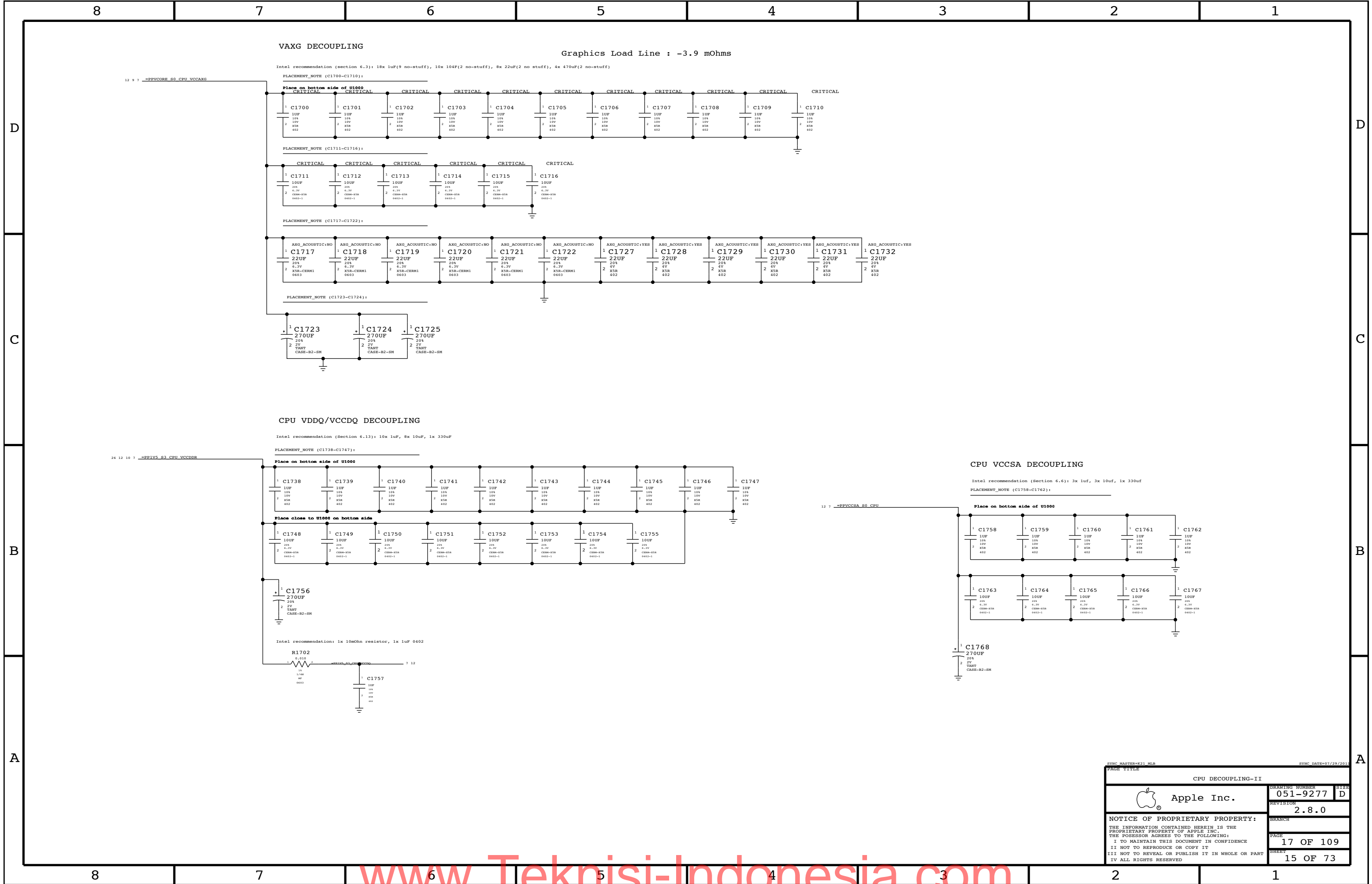








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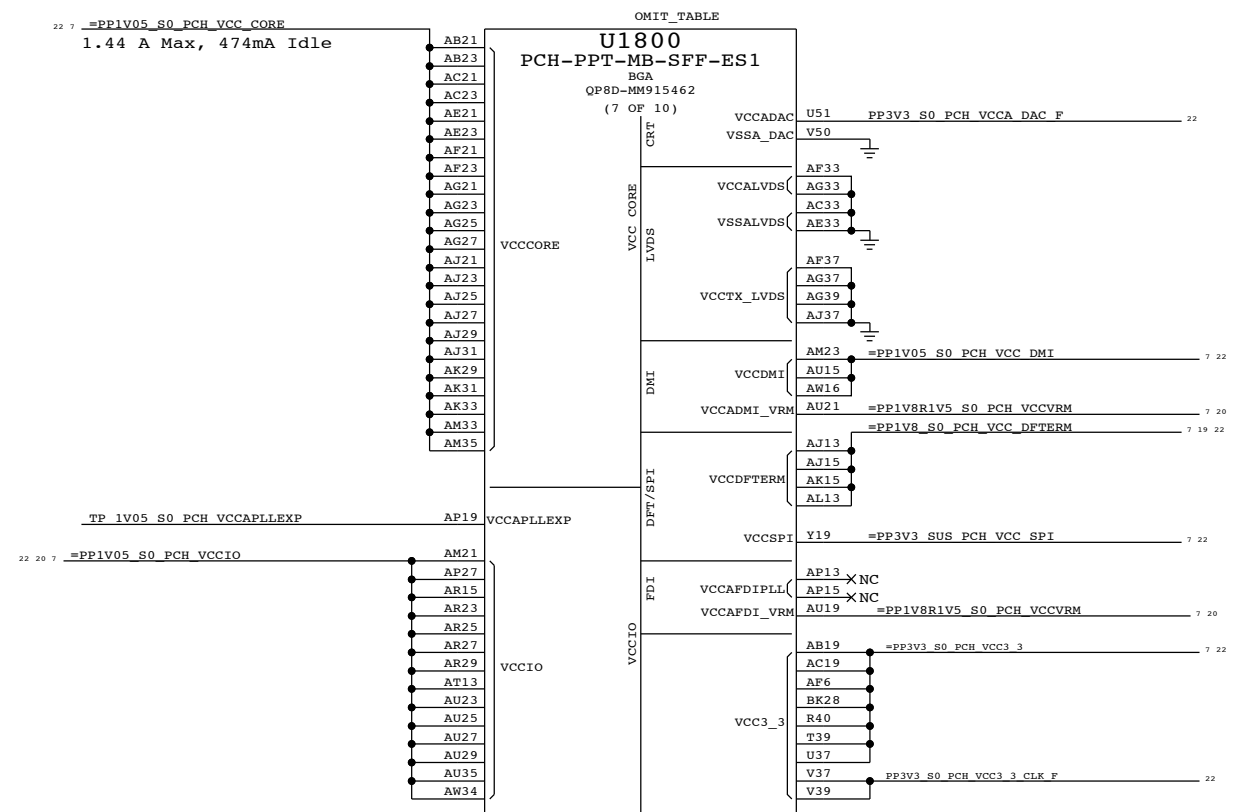
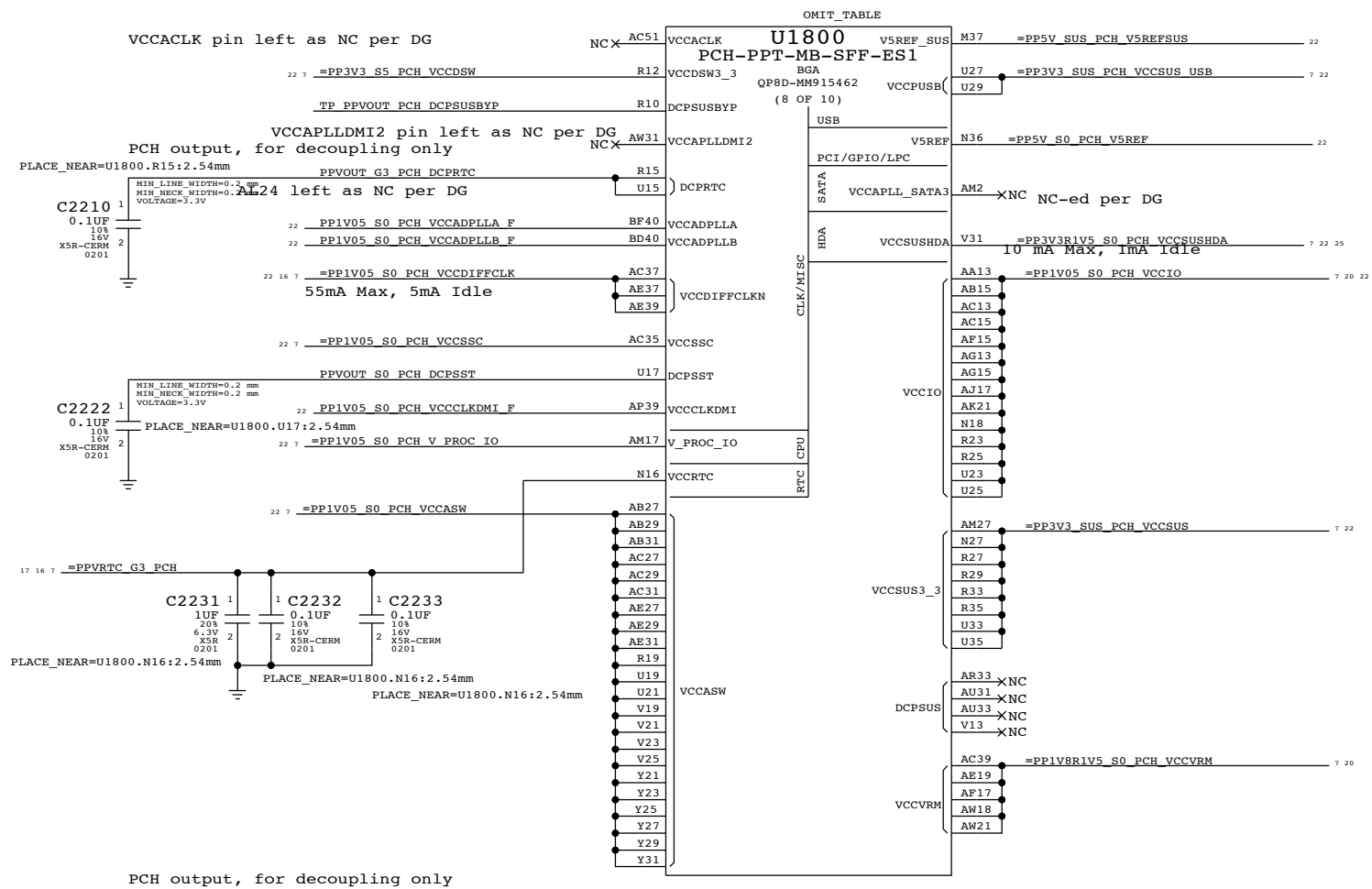


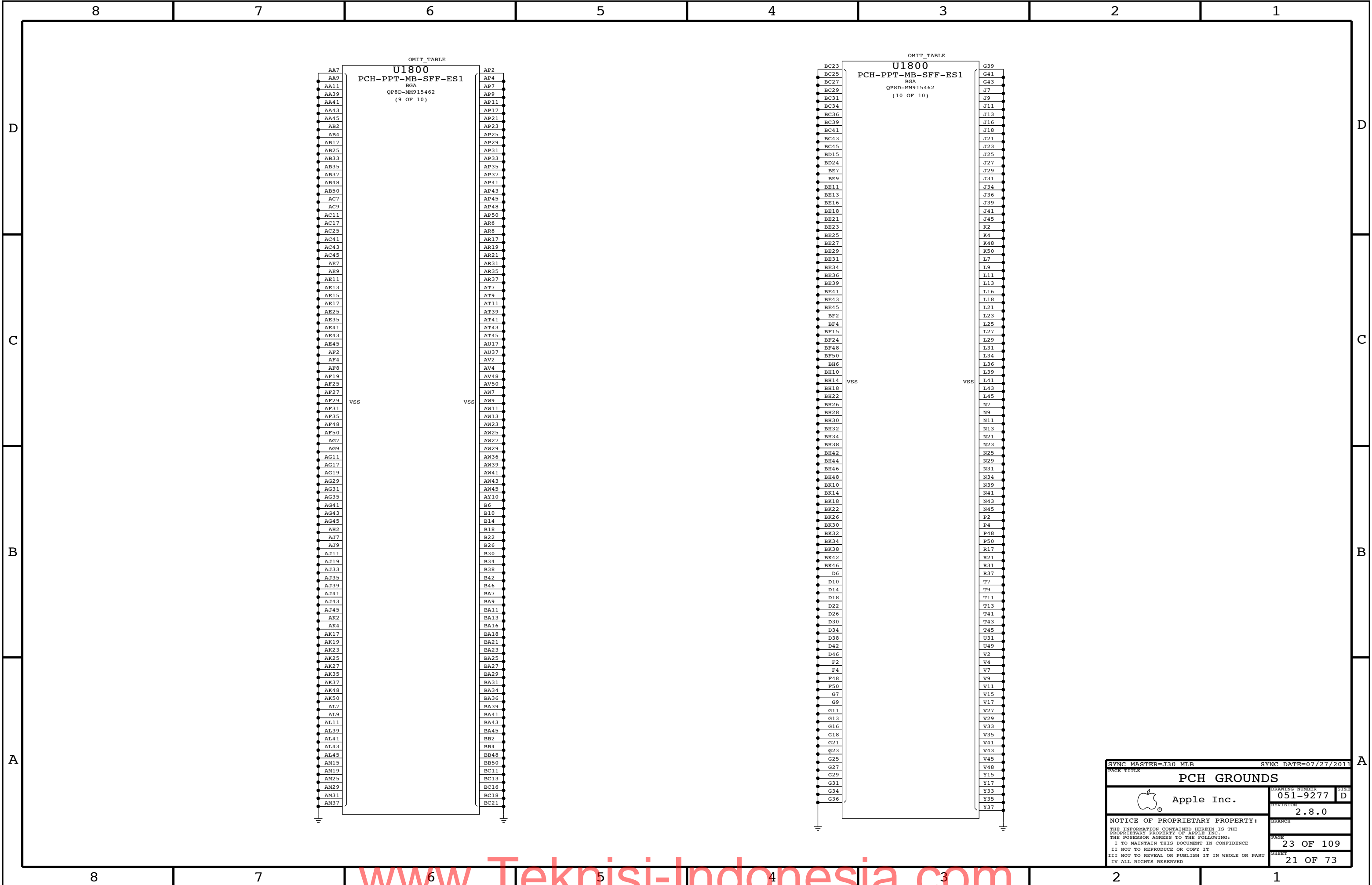













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SYNC DATE=07/27/2011

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PCH GROUNDS

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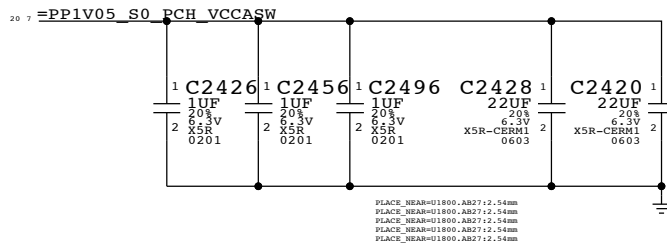
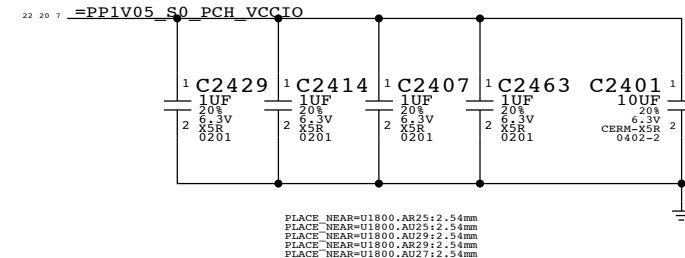
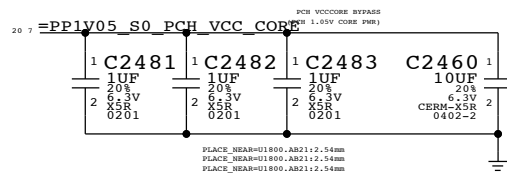
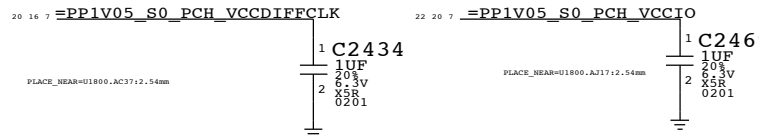
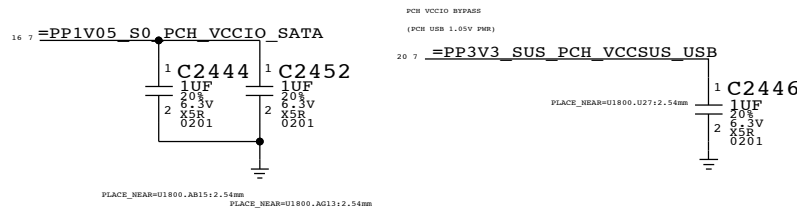
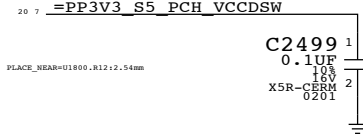
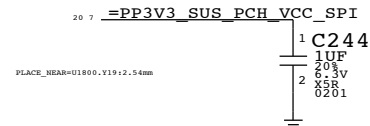
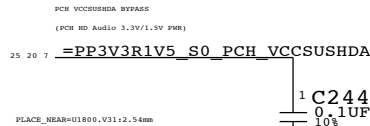
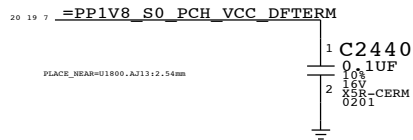
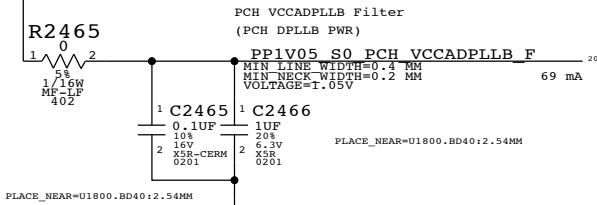
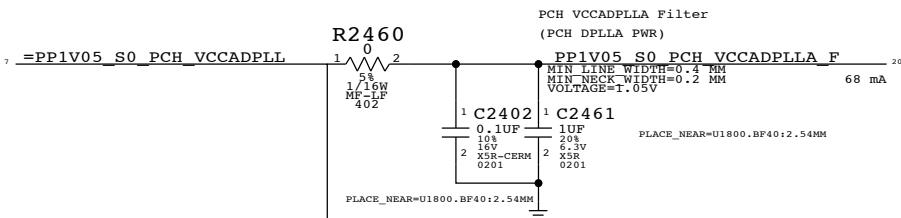
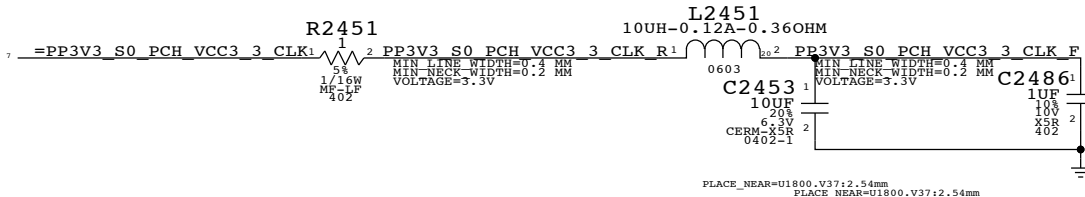
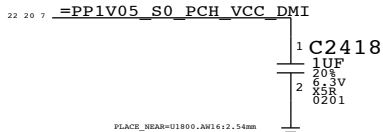
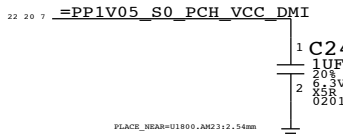
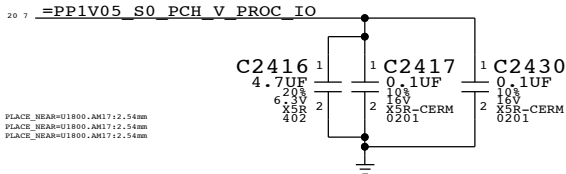
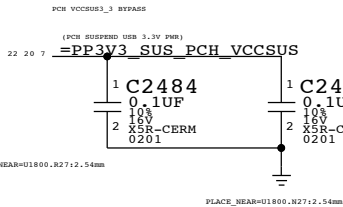
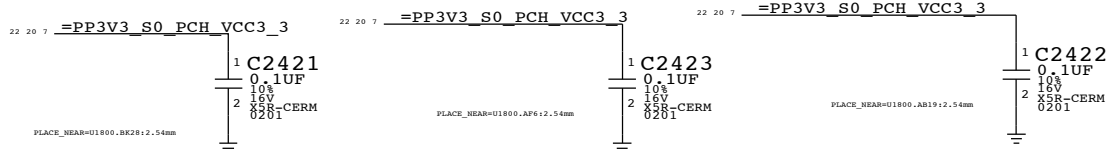
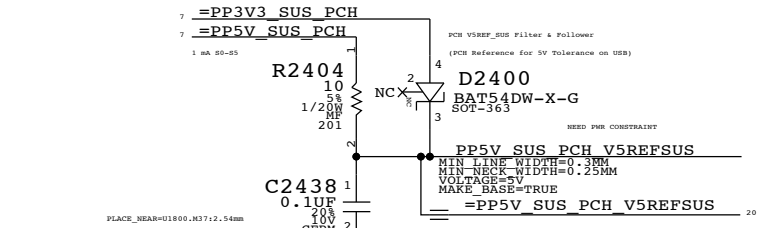
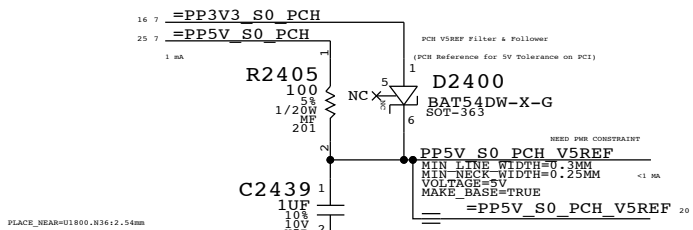
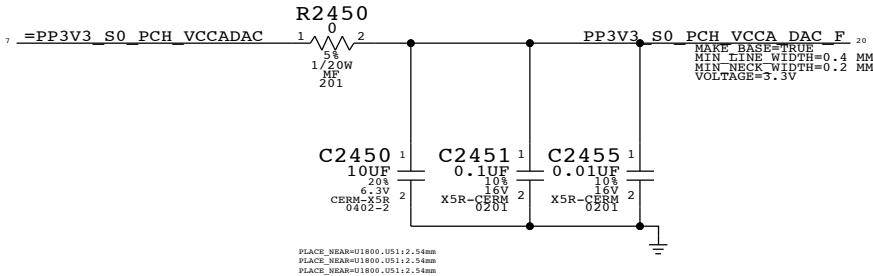
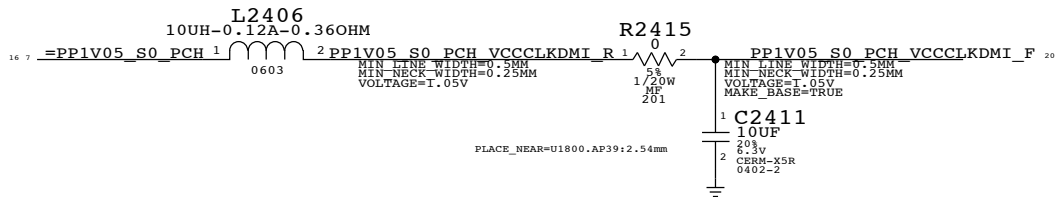
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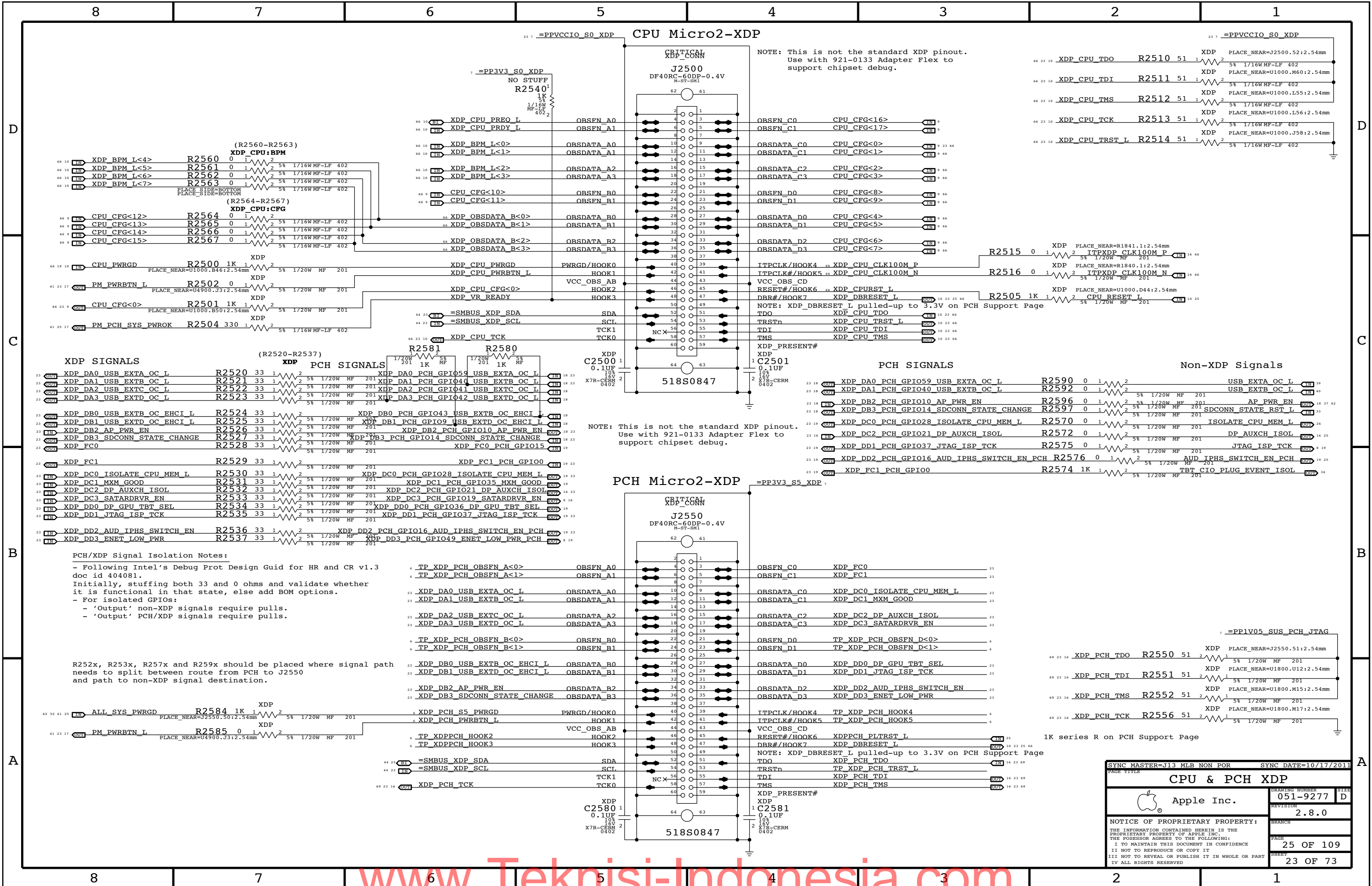
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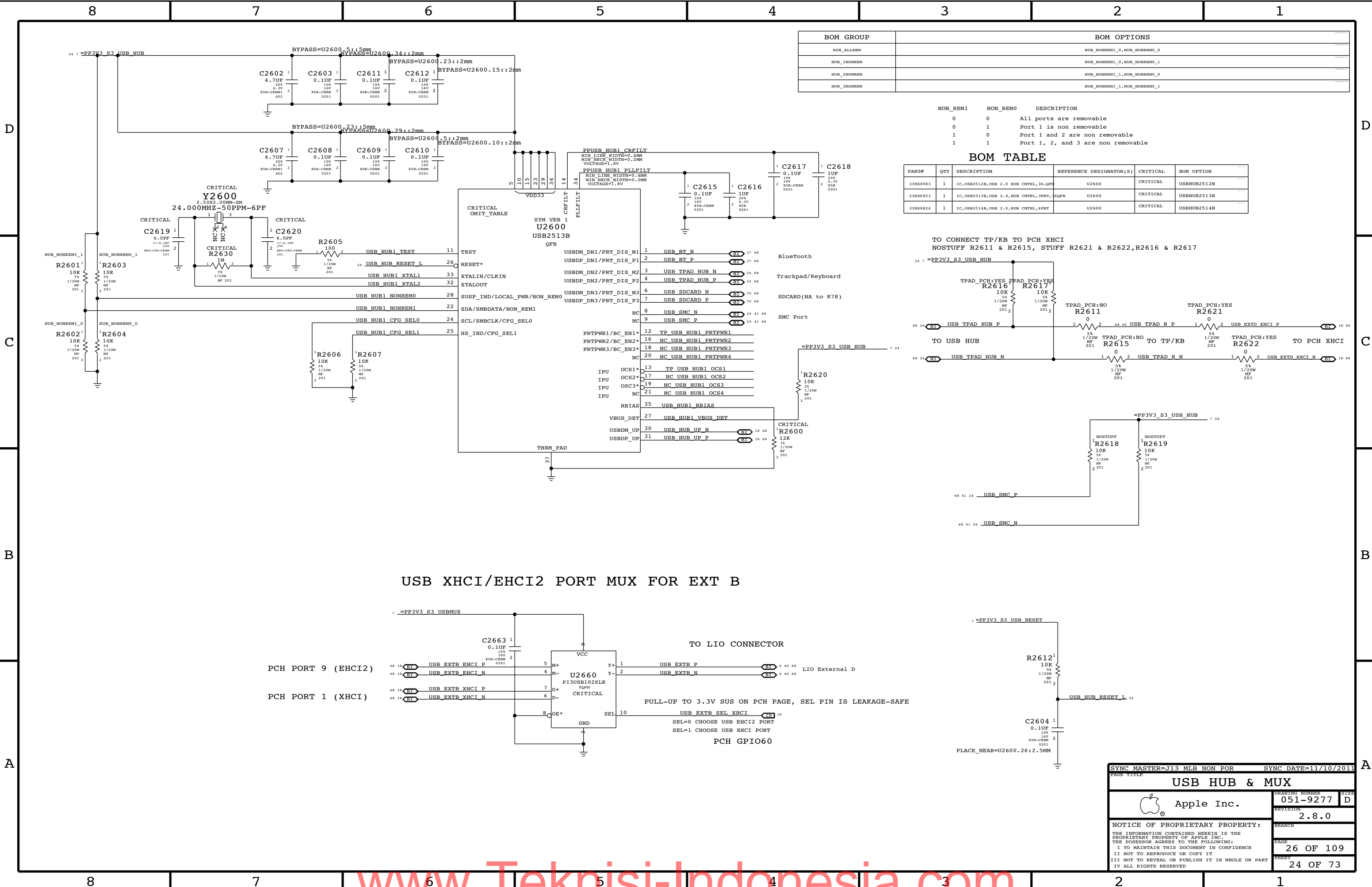
B

A



PAGE TITLE		PAGE NUMBER	
PCH DECOUPLING		051-9277	
Apple Inc.		2.8.0	
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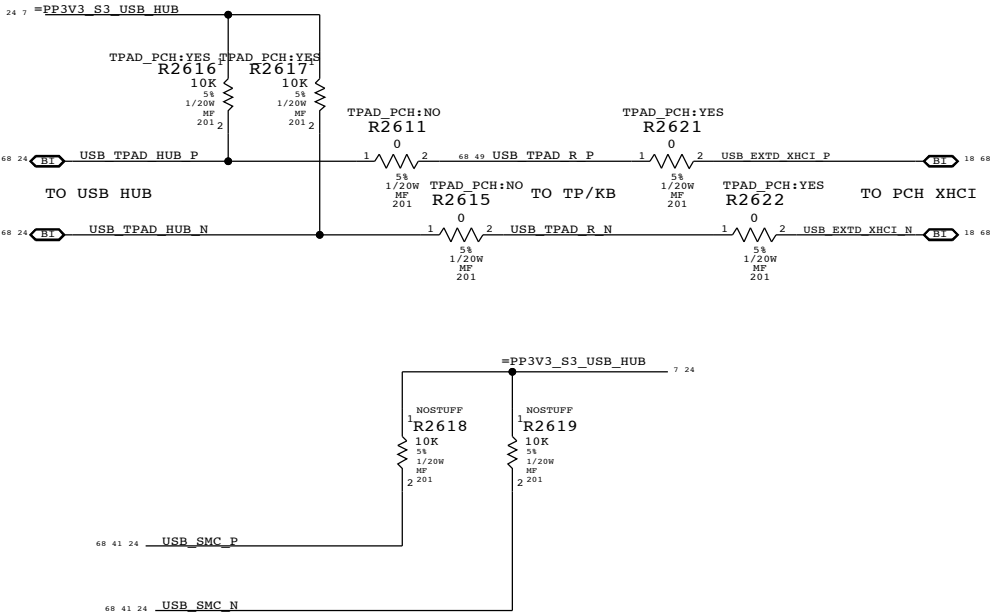
BOM GROUP	BOM OPTIONS
HUB_ALLREM	HUB_NONREM1_0,HUB_NONREM0_0
HUB_1NONREM	HUB_NONREM1_0,HUB_NONREM0_1
HUB_2NONREM	HUB_NONREM1_1,HUB_NONREM0_0
HUB_3NONREM	HUB_NONREM1_1,HUB_NONREM0_1

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

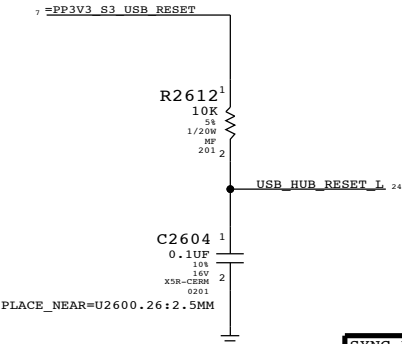
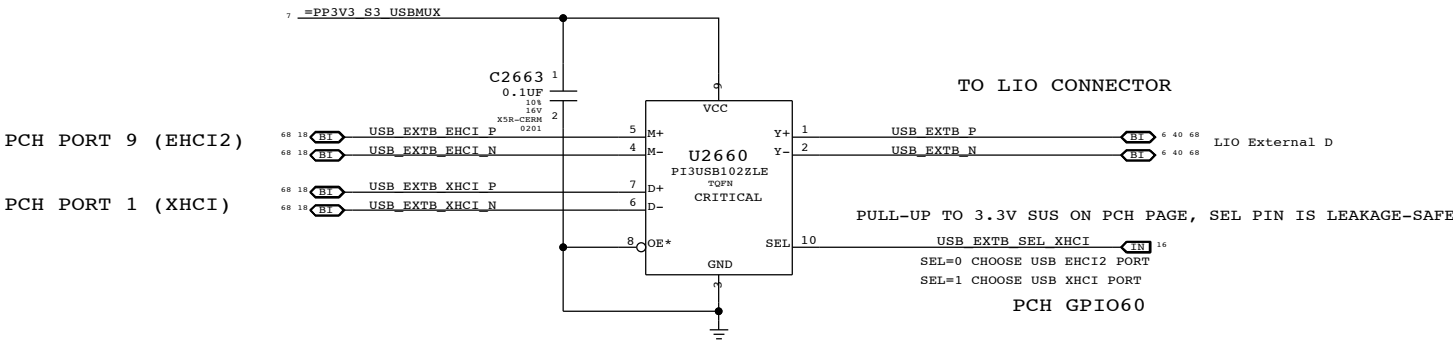
BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0983	1	IC,USB2512B,USB 2.0 HUB CNTRL,36-QFN	U2600	CRITICAL	USBHUB2512B
338S0923	1	IC,USB2513B,USB 2.0,HUB CNTRL,3PRT,46QFN	U2600	CRITICAL	USBHUB2513B
338S0824	1	IC,USB2514B,USB 2.0,HUB CNTRL,4PRT	U2600	CRITICAL	USBHUB2514B

TO CONNECT TP/KB TO PCH XHCI  
NOSTUFF R2611 & R2615, STUFF R2621 & R2622,R2616 & R2617

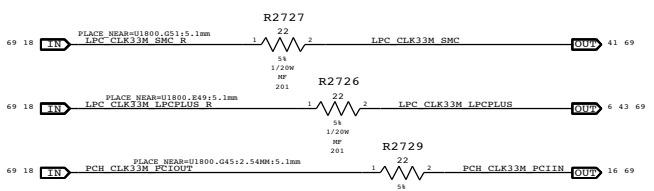
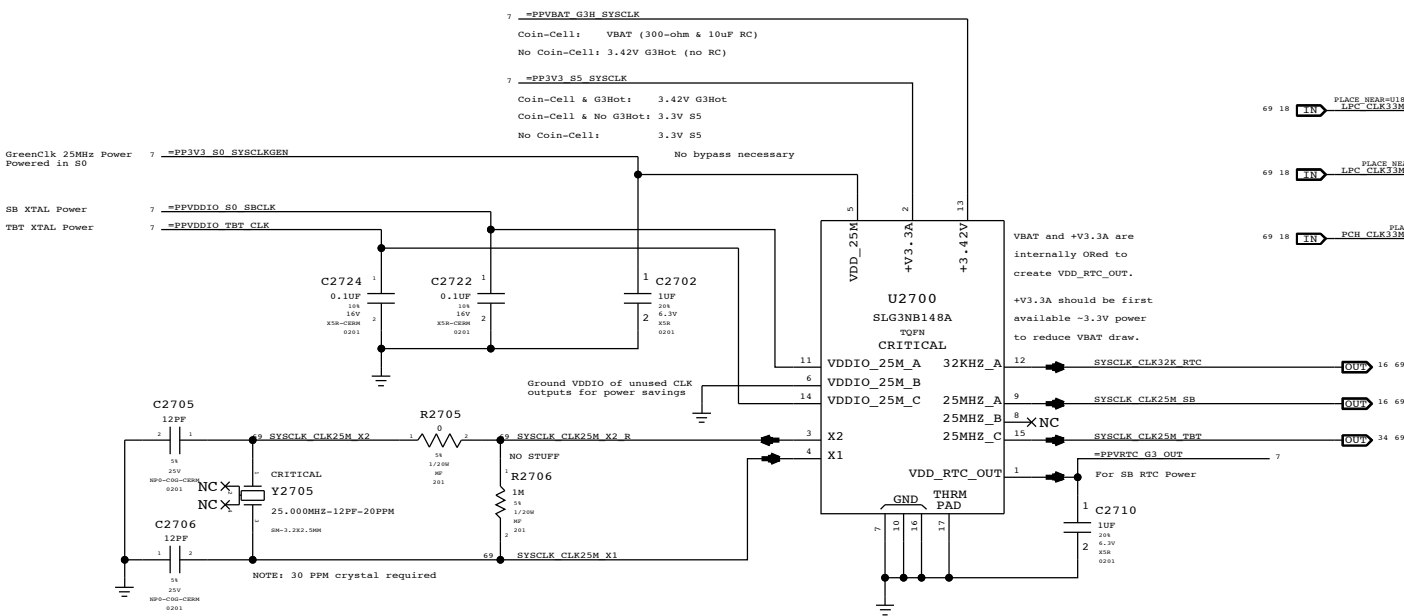


USB XHCI/EHCI2 PORT MUX FOR EXT B



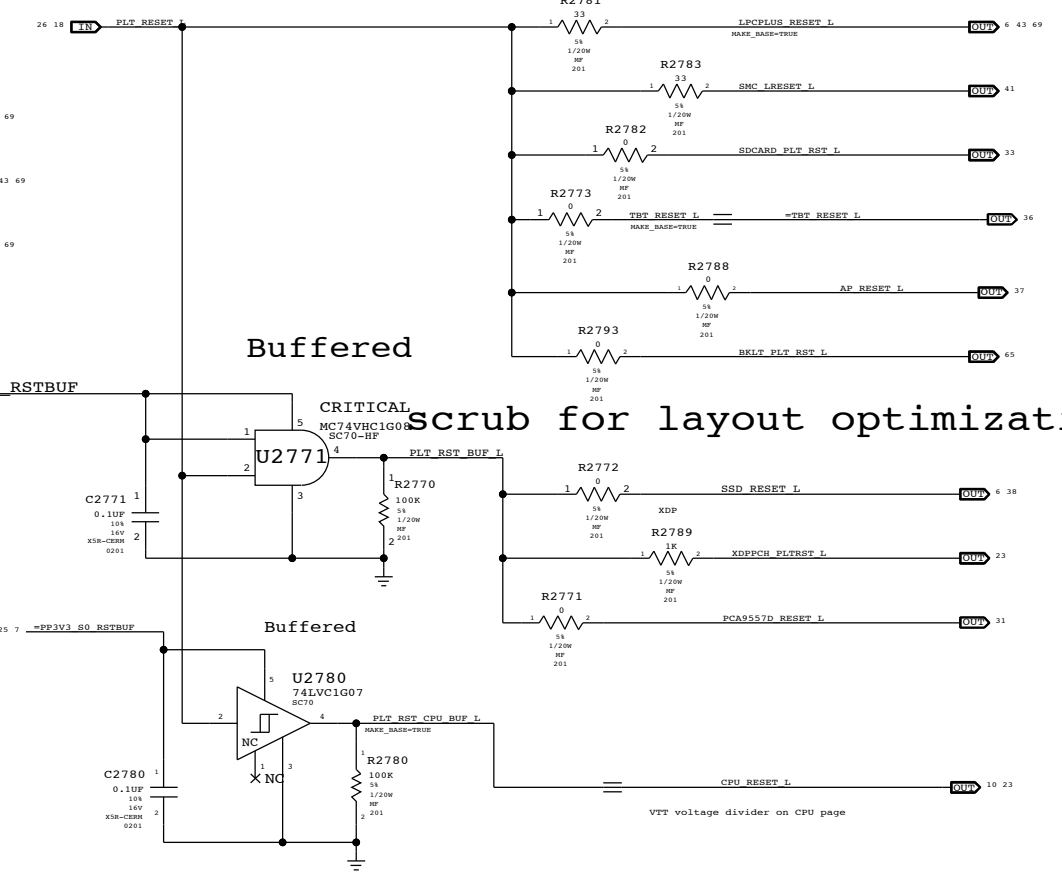
PAGE TITLE		SYNC MASTER=J13 MLB NON POR		SYNC DATE=11/10/2011	
USB HUB & MUX		DRAWING NUMBER		SIZE	
Apple Inc.		051-9277		D	
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System RTC Power Source & 32kHz / 25MHz Clock Generator

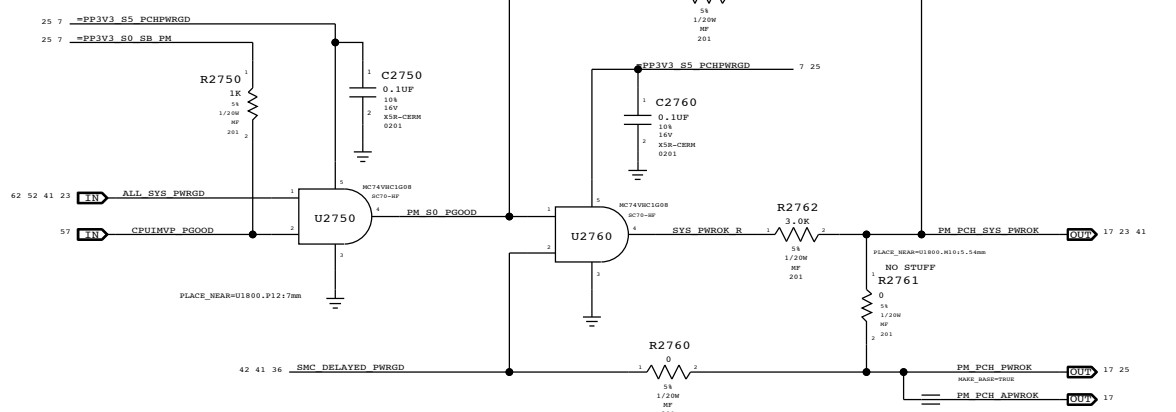


Platform Reset Connections  
Unbuffered

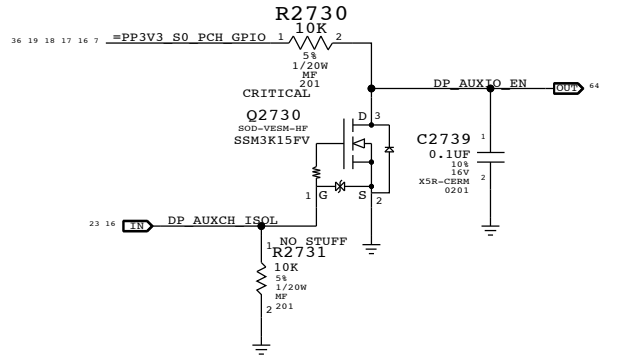
Buffered



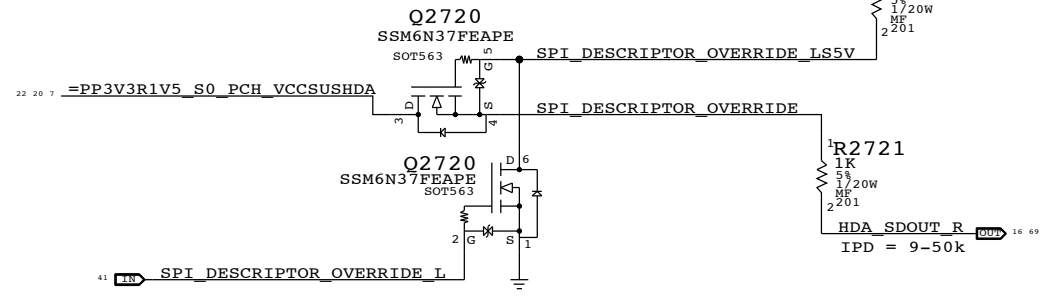
PCH S0 PWRGD



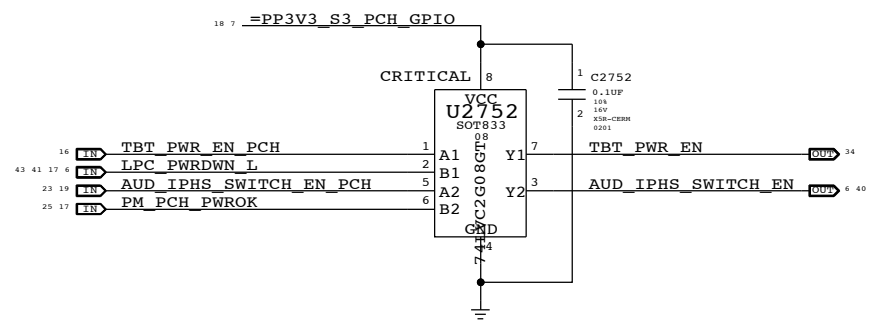
DP\_AUXIO\_EN Inversion



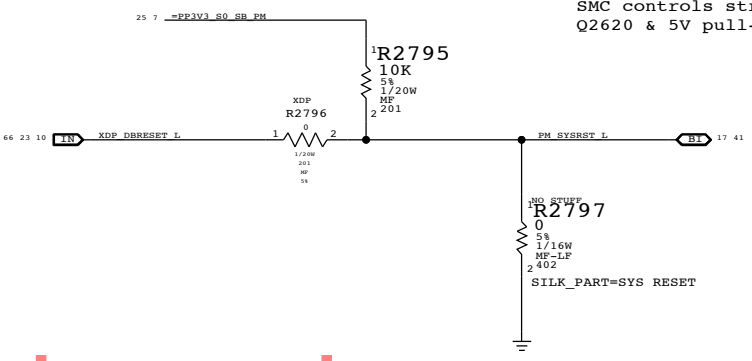
PCH ME Disable Strap




GPIO Glitch Prevention



PCH Reset Button



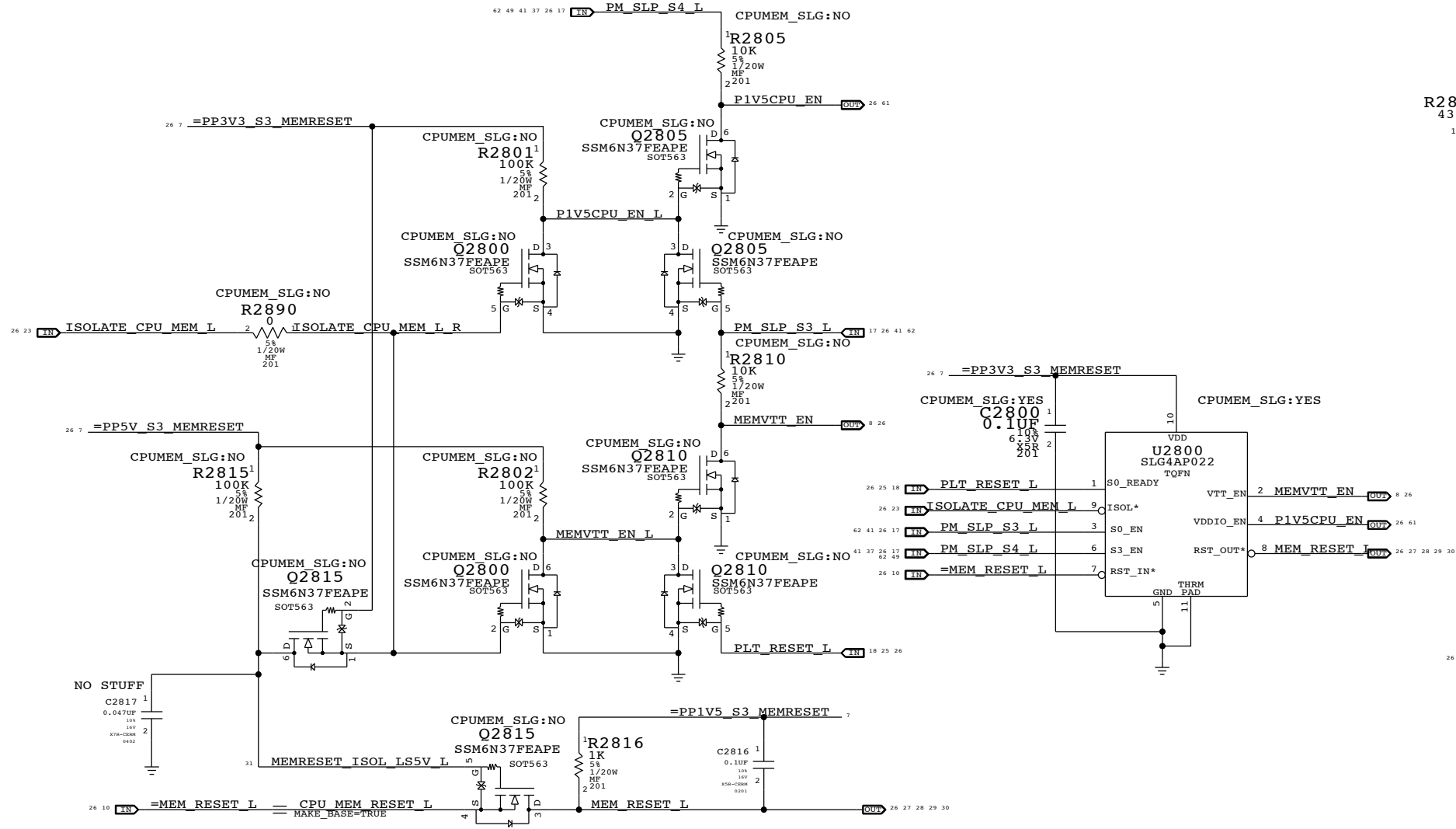
PCH uses HDA\_SDO as a power-up strap. If low, ME functions normally. If high, ME is disabled. This allows for full re-flashing of SPI ROM. SMC controls strap enable to allow in-field control of strap setting. Q2620 & 5V pull-up allows circuit to work regardless of HDA voltage.

SYM WATER-021.HLS		ESD DATE=07/28/2011	
PAGE TITLE			
Clock (CK505) and Chipset Support			
		DRAWING NUMBER	SIZE
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		REVISION	
		2.8.0	
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		BRANCH	
		PAGE	
		27 OF 109	
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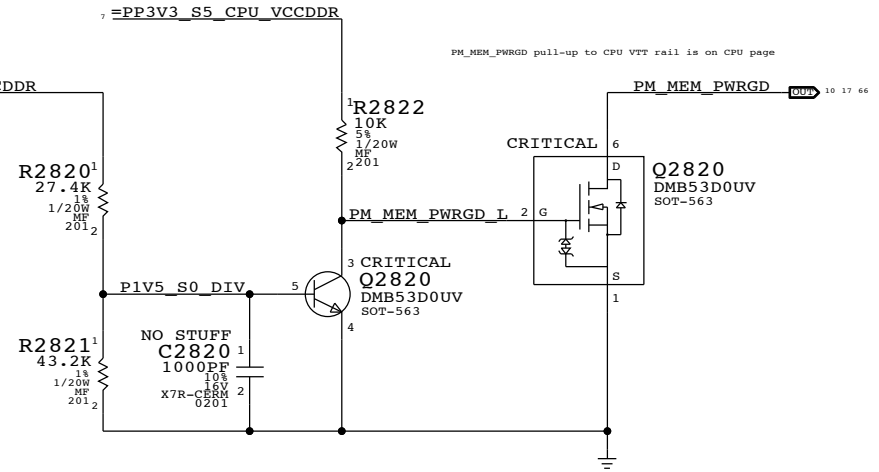
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM\_DRAMRST# output from the S0-DIMMs when necessary.

ISOLATE\_CPU\_MEM\_L GPIO state during S3->S0 transitions determines behavior of signals.  
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM\_RESET\_L not isolated.  
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM\_RESET\_L isolated.

P1V5CPU\_EN = (ISOLATE\_CPU\_MEM\_L + PM\_SLP\_S3\_L) \* PM\_SLP\_S4\_L  
MEMVTT\_EN = (ISOLATE\_CPU\_MEM\_L + PLT\_RST\_L) \* PM\_SLP\_S3\_L  
MEM\_RESET\_L = !ISOLATE\_CPU\_MEM\_L + CPU\_MEM\_RESET\_L

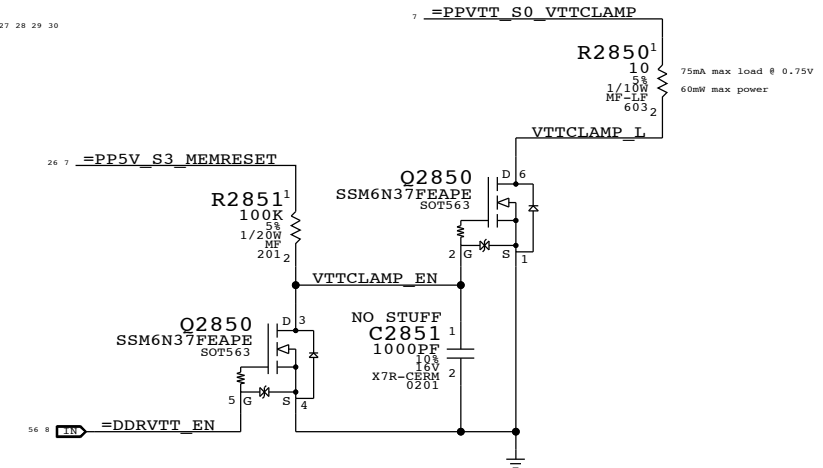


### 1V5 S0 "PGOOD" for CPU



### MEMVTT Clamp


Ensures CKE signals are held low in S3



Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1	1
2	0	0	0	1	1	0	0	0
3	0	0	0	1	X	0	0	0
S3	4	0	0	1	X	0	0	1
to	5	0	1	1	0 (*)	1	1	1
6	0	1	1	1	1	1	1	1
S0	7	1	1	1	1	CPU_MEM_RESET_L	1	1

(\*) CPU\_MEM\_RESET\_L asserts due to loss of PM\_MEM\_PWRGD, must wait for software to clear before deasserting ISOLATE\_CPU\_MEM\_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE\_CPU\_MEM\_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM\_RESET\_L will not properly assert. Software must deassert ISOLATE\_CPU\_MEM\_L and then generate a valid reset cycle on CPU\_MEM\_RESET\_L.

CPU WATTS=213 M16 M10N P0R		SYSC DATE=11/19/2011	
PAGE TITLE			
CPU Memory S3 Support		DRAWING NUMBER	SIZE
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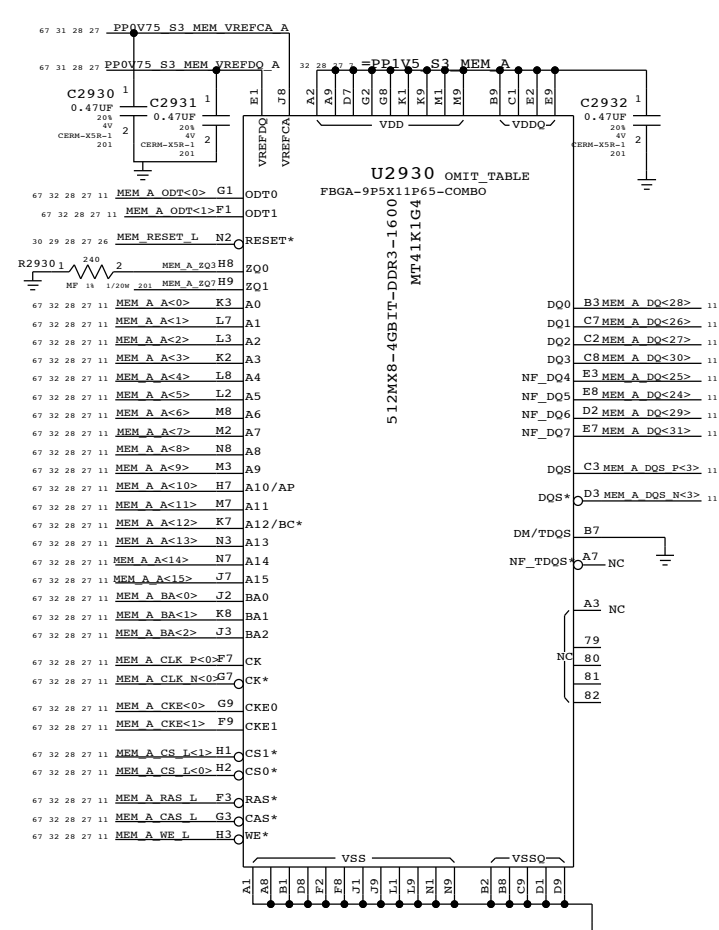
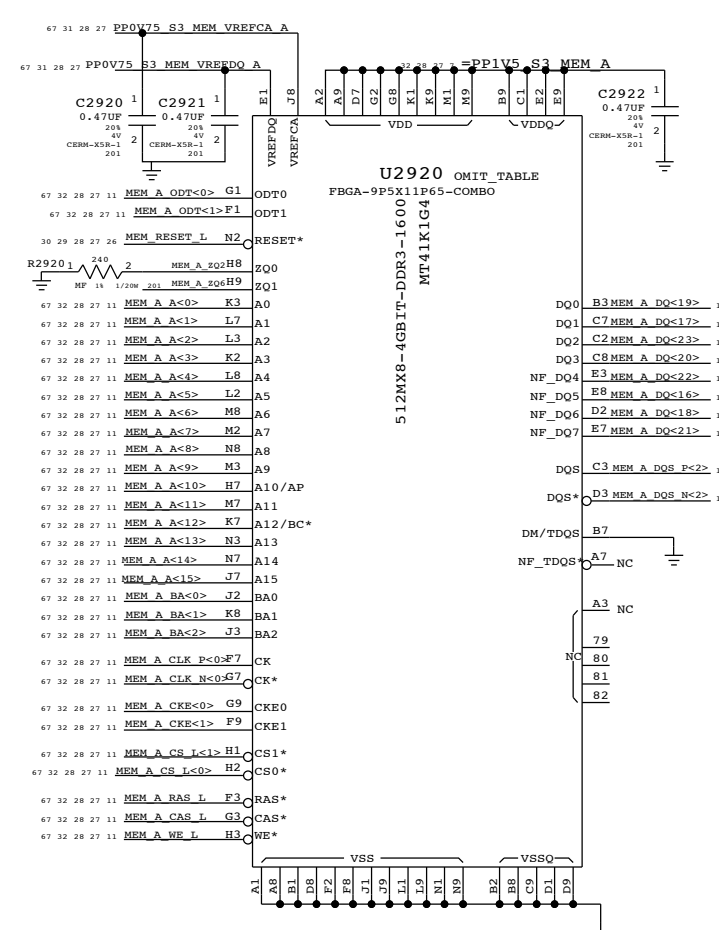
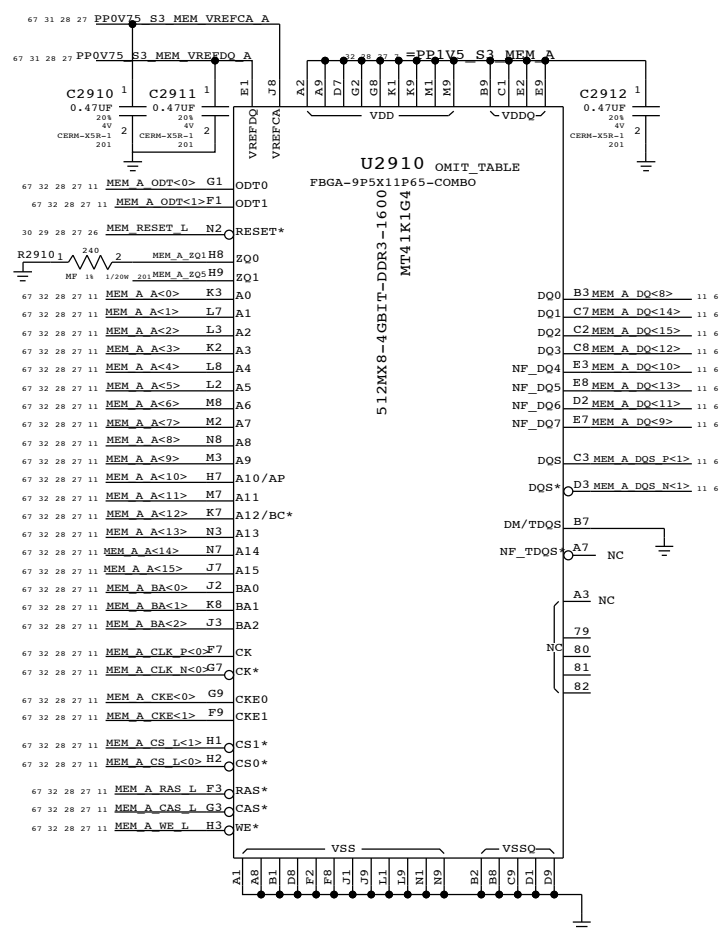
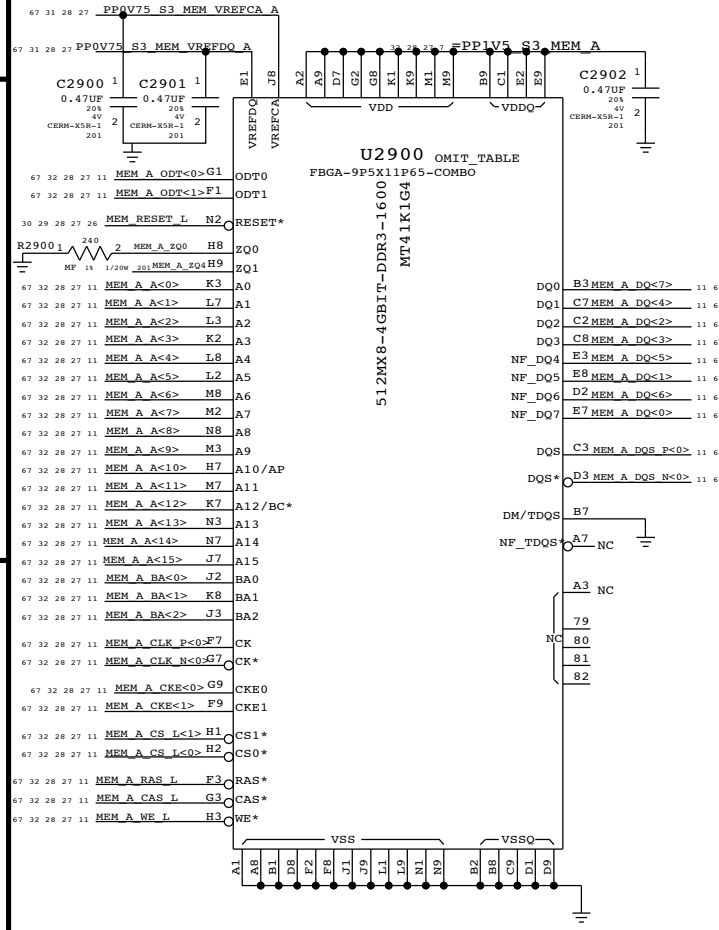
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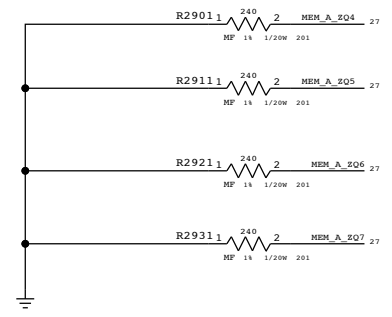
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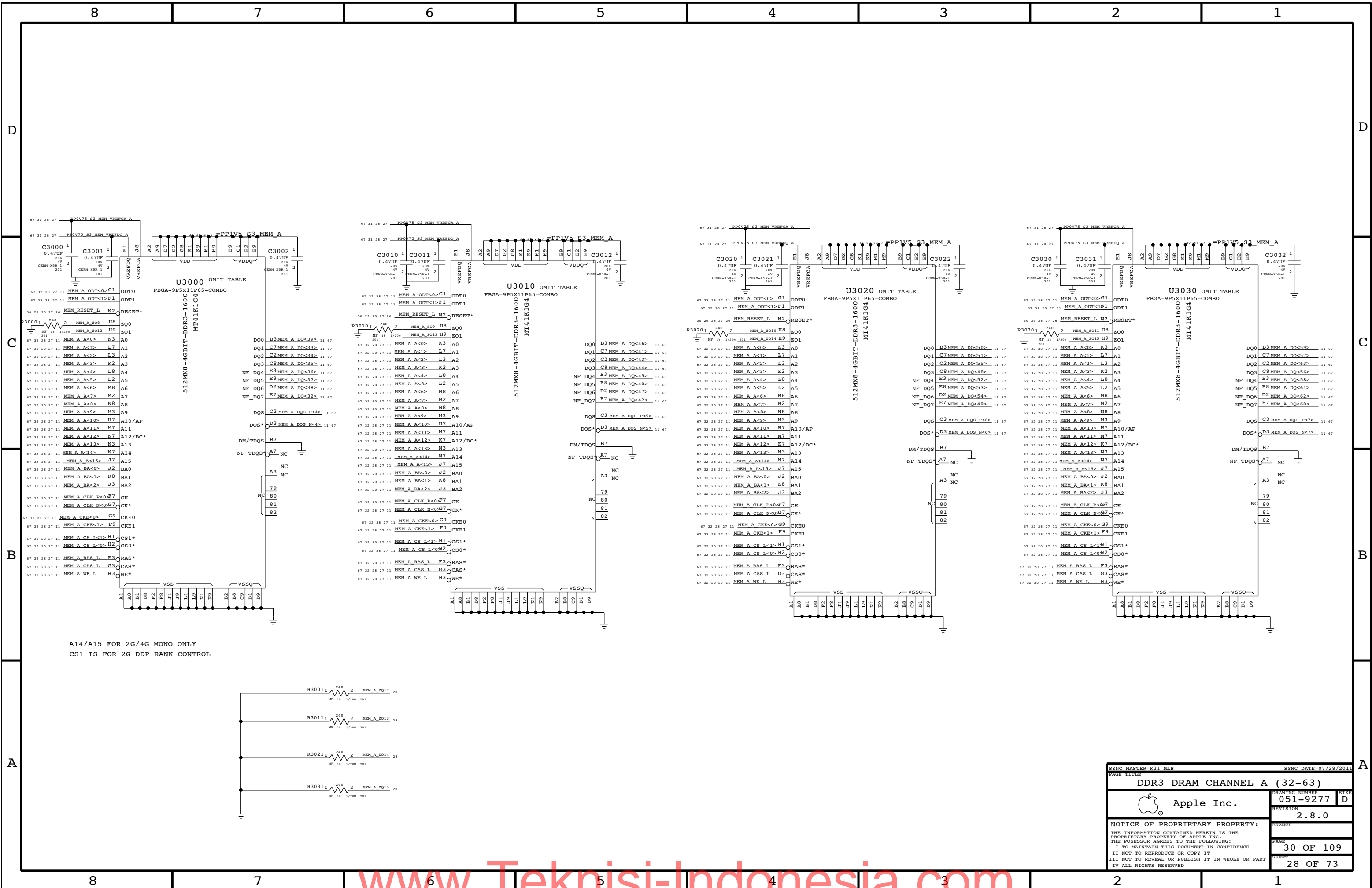


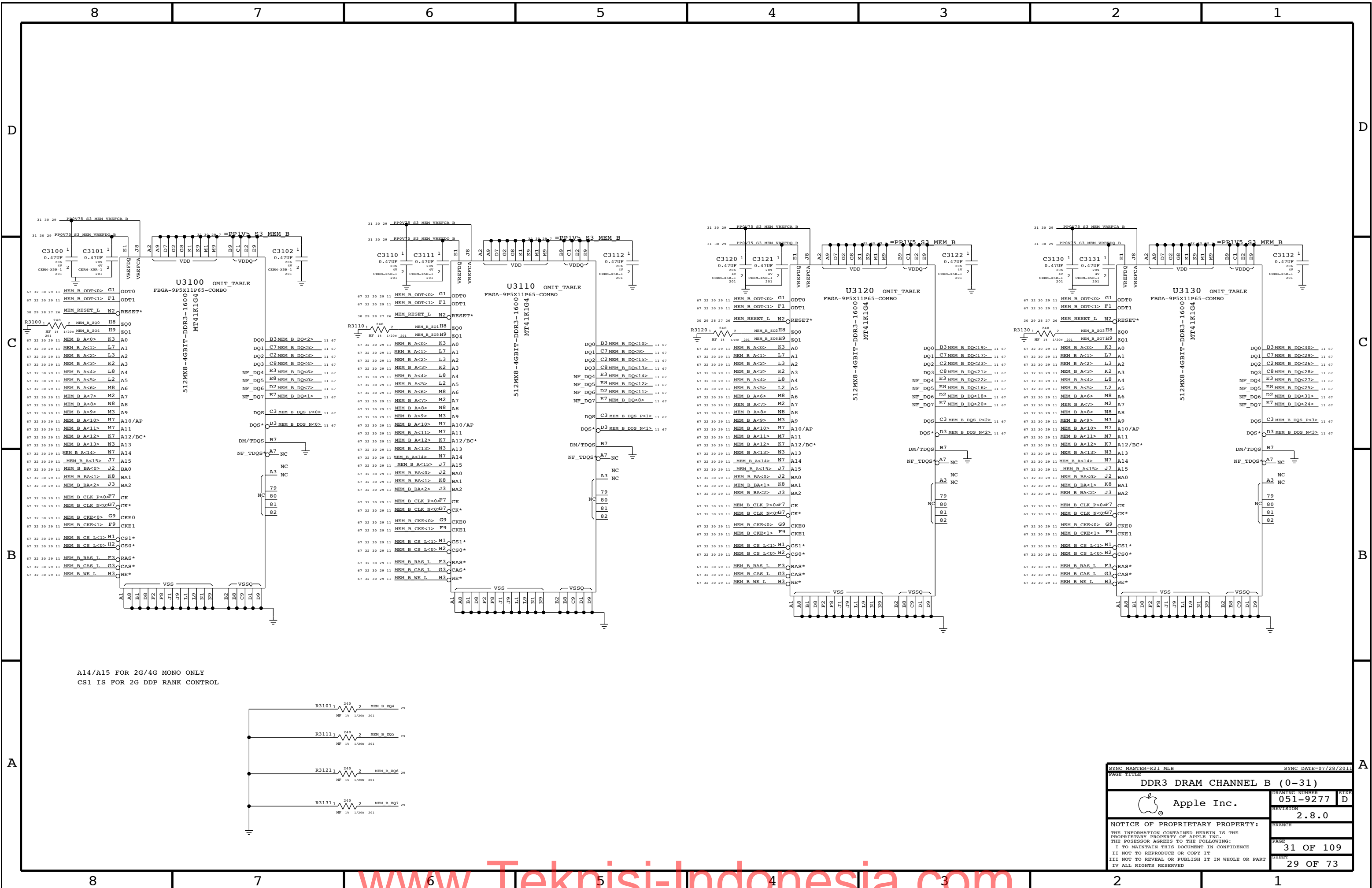
A14/A15 FOR 2G/4G MONO ONLY


CS1 IS FOR 2G DDP RANK CONTROL

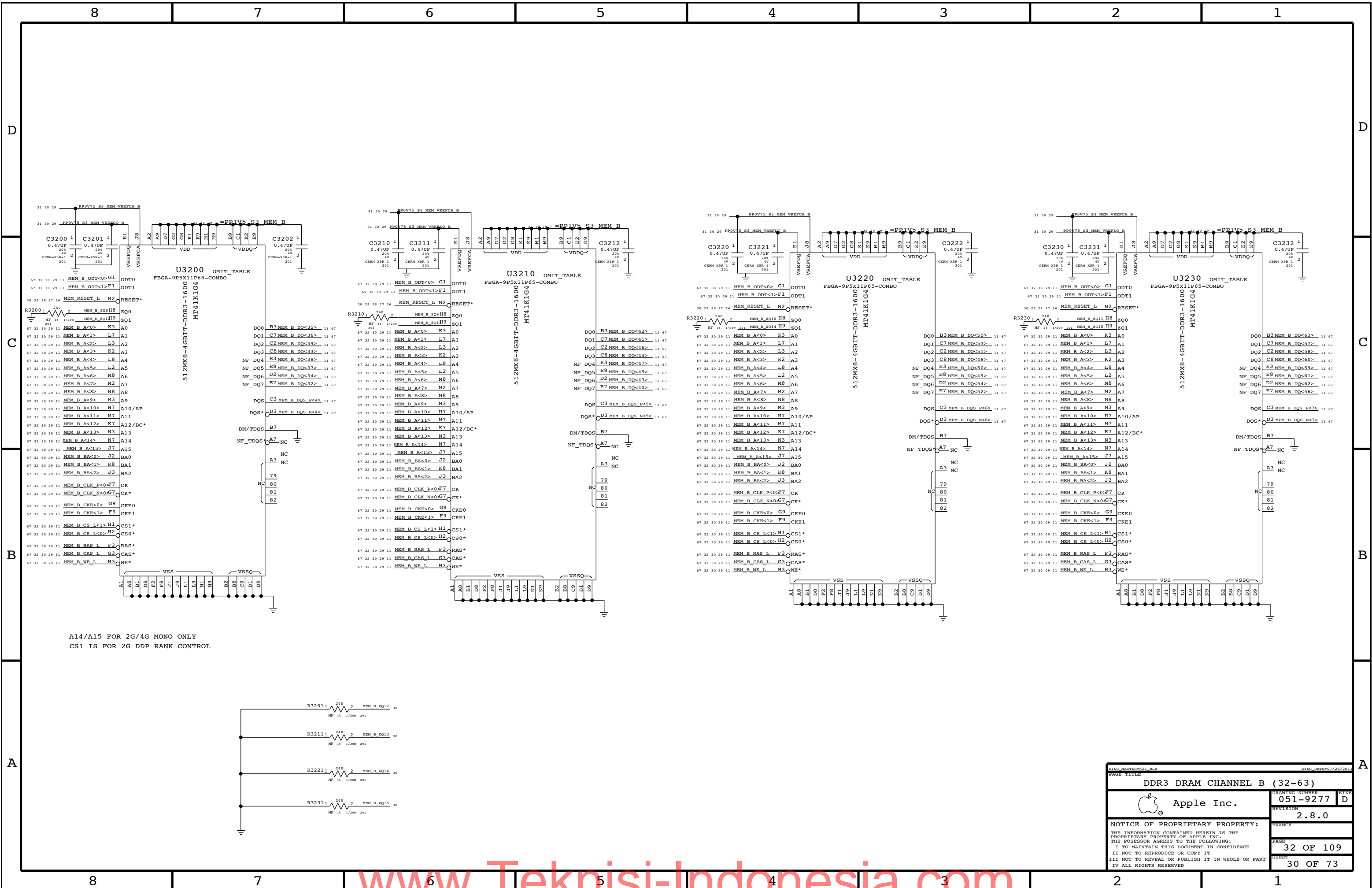



SYNC MASTER=K21 MLB		SYNC DATE=07/28/2011	
PAGE TITLE			
DDR3 DRAM CHANNEL A (0-31)			
 Apple Inc.	DRAWING NUMBER	051-9277	SIZE D
	REVISION	2.8.0	
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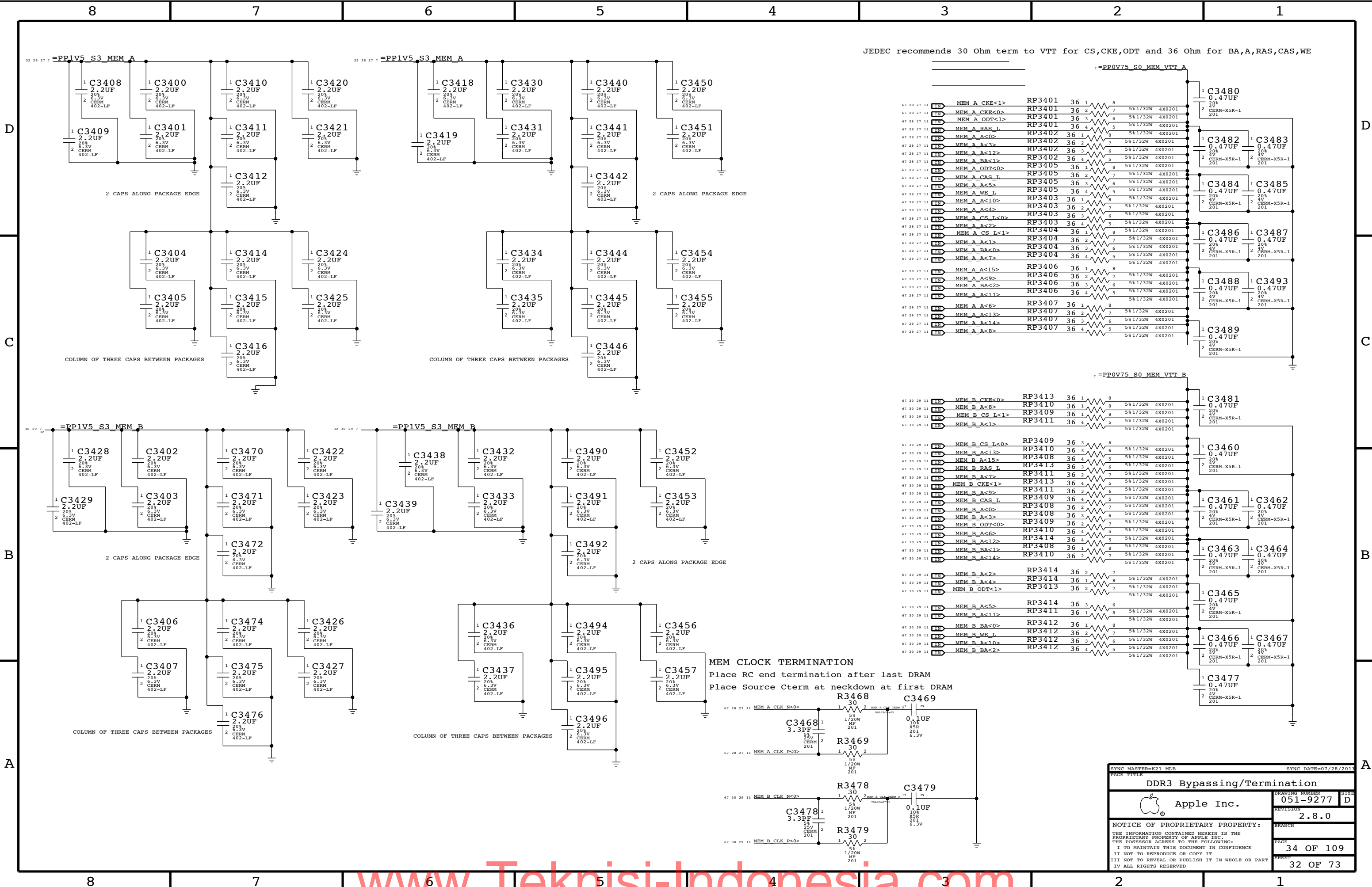


SYNC MASTER=K21 MLB		SYNC DATE=07/28/2011	
PAGE TITLE			
DDR3 DRAM CHANNEL B (0-31)			
 Apple Inc.	DRAWING NUMBER	051-9277	SIZE D
	REVISION	2.8.0	
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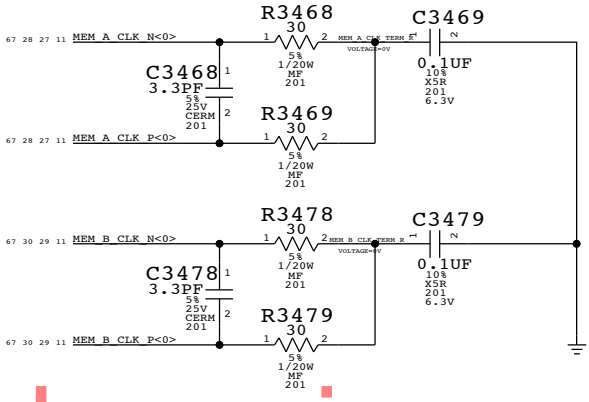
SYNCHARTER#21.MEM		SYNCHARTER#21.MEM	
PAGE TITLE			
DDR3 DRAM CHANNEL B (32-63)		DRAWING NUMBER	
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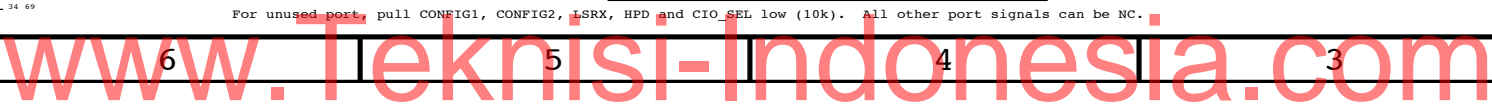
JEDEC recommends 30 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE

**MEM CLOCK TERMINATION**  
Place RC end termination after last DRAM  
Place Source Cterm at neckdown at first DRAM



SYNC MASTER=K21 MEB		SYNC DATE=07/28/2011	
PAGE TITLE			
DDR3 Bypassing/Termination			
	Apple Inc.	DRAWING NUMBER	051-9277
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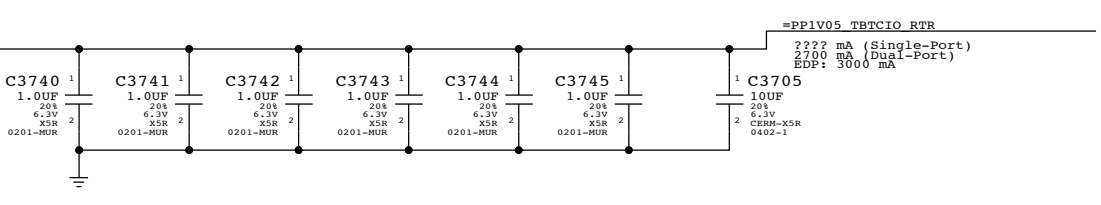
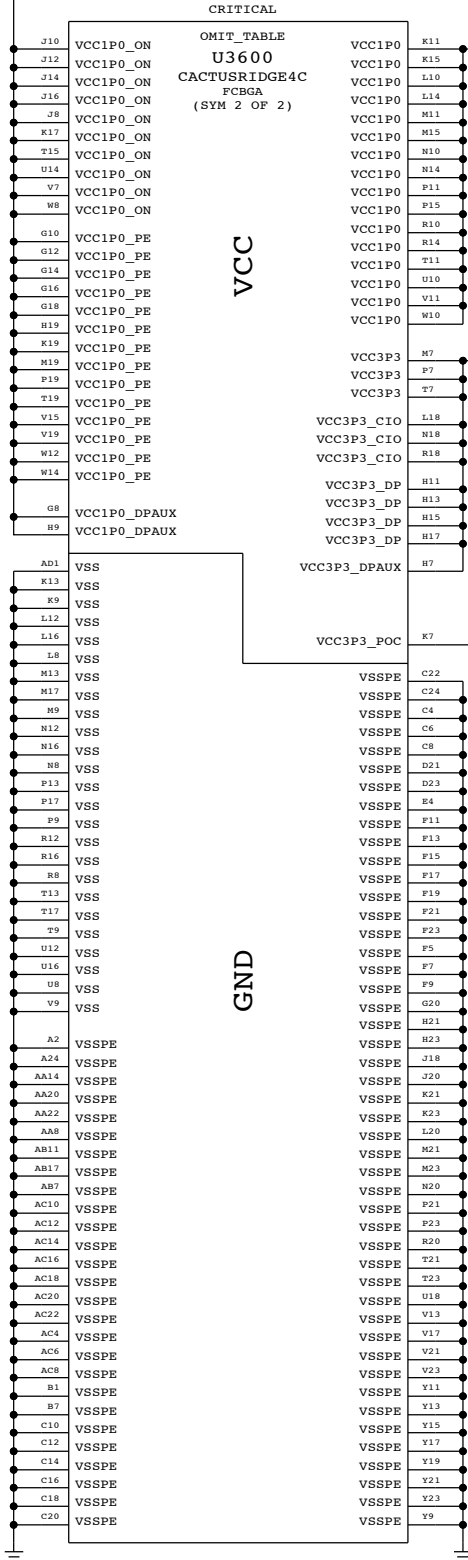
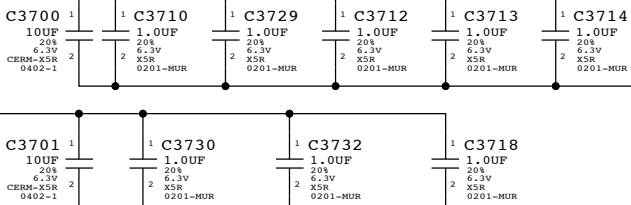
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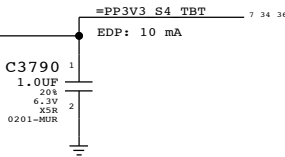
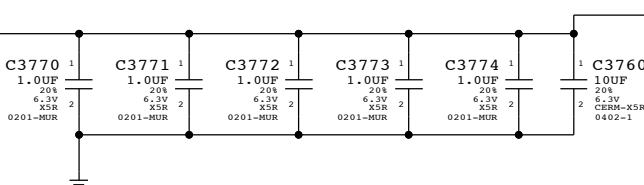
B


A

=PP1V05\_TBTLIC\_RTR  
???? mA (Single Port)  
250 mA (Dual Port)  
EDP: 1000 mA



=PP3V3\_TBTLIC\_RTR : 34 36  
??? mA (Single-Port)  
250 mA (Dual-Port)  
EDP: 240 mA



SYNC MASTER=J11 MLB		SYNC DATE=10/04/2011	
PAGE TITLE			
Thunderbolt Host (2 of 2)			
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## Page Notes

Power aliases required by this page:

- =PPVIN\_SW\_TBTBST (8-13V Boost Input)
- =PP18V\_TBT\_REG (18V Boost Output)
- =PP3V3\_TBT\_P3V3TBTFTET (3.3V FET Input)
- =PP3V3\_TBT\_FET (3.3V FET Output)
- =PP3V3\_S0\_TBTFWRCTL
- =PP1V05\_TBT\_P1V05TBTFTET (1.05V FET Input)
- =PP1V05\_TBT\_FET (1.05V FET Output)

Signal aliases required by this page:

- =TBT\_CLKREQ\_L
- =TBT\_RESET\_L

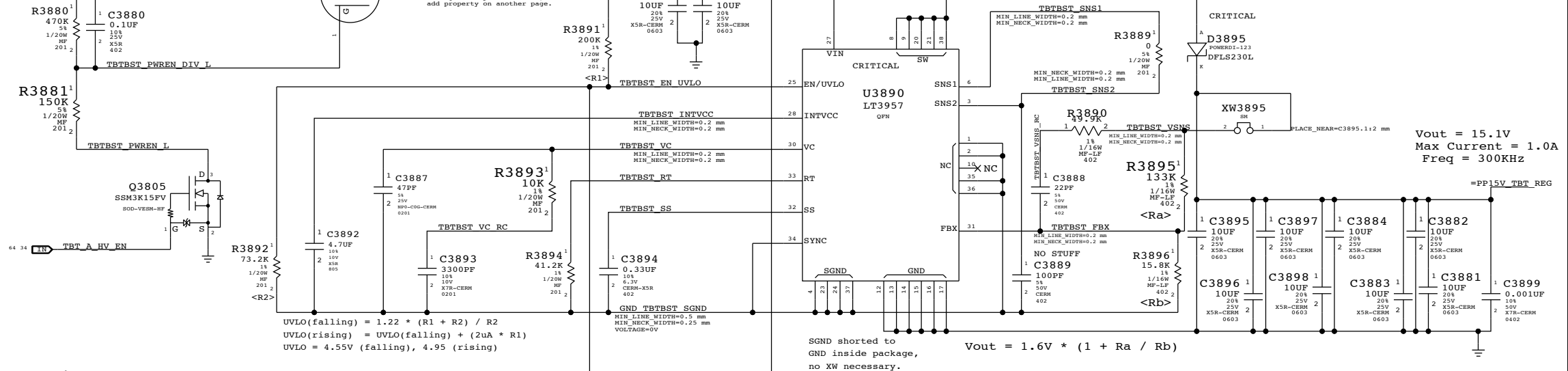
BOM options provided by this page:

TBTBST:Y - Stuffs 18V boost circuitry.

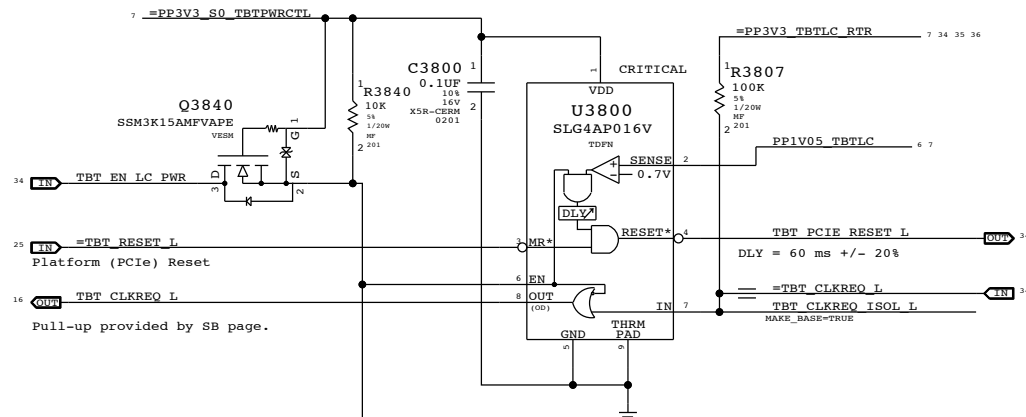
## TBT 15V Boost Regulator

SI8409DB:  
Vds(max): -30V  
Vgs(max): +/-12V  
Vgs(th): -1.4V  
Rds(on): 46mOhm @ 4.5V Vgs  
Id(max): 3.7A @ 70C

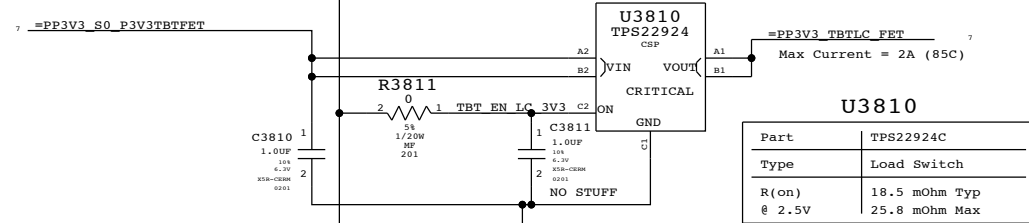
=PPVIN\_SW\_TBTBST  
8-13V Input  
Changes required  
for 2S.



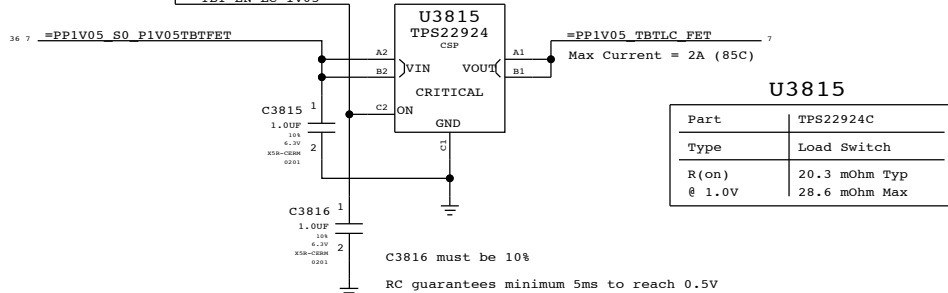
## Supervisor & CLKREQ# Isolation



## 3.3V TBT "LC" Switch

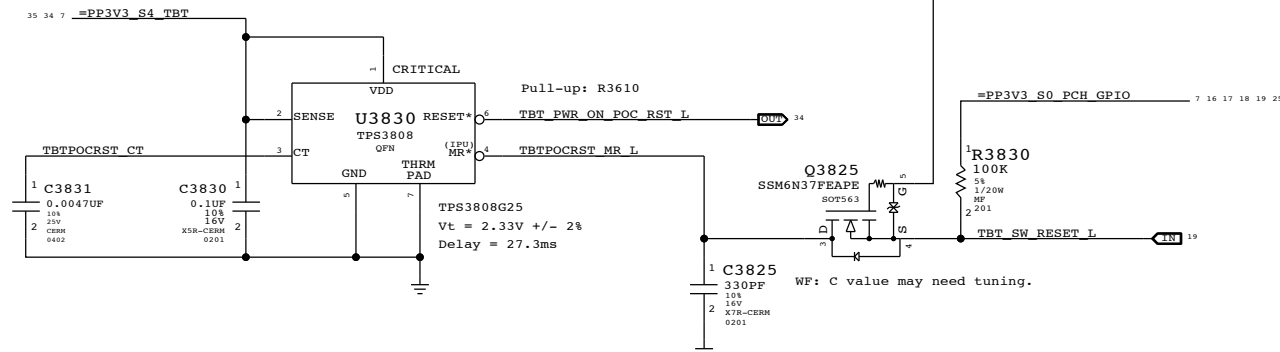


## 1.05V TBT "LC" Switch

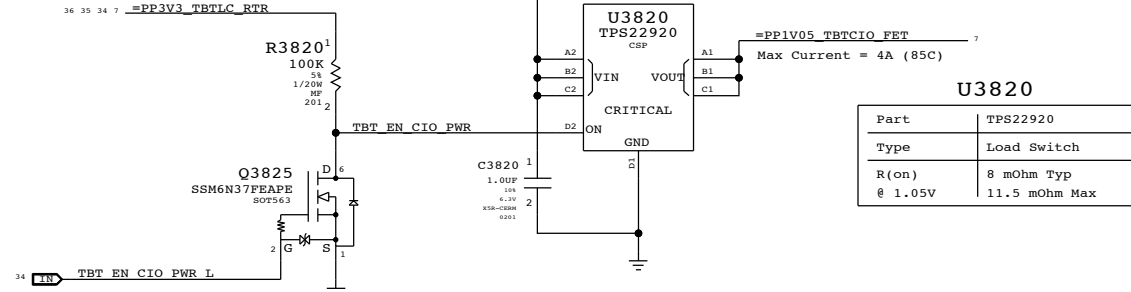


## TBT "POC" Power-up Reset

Intel investigating whether RC is sufficient.

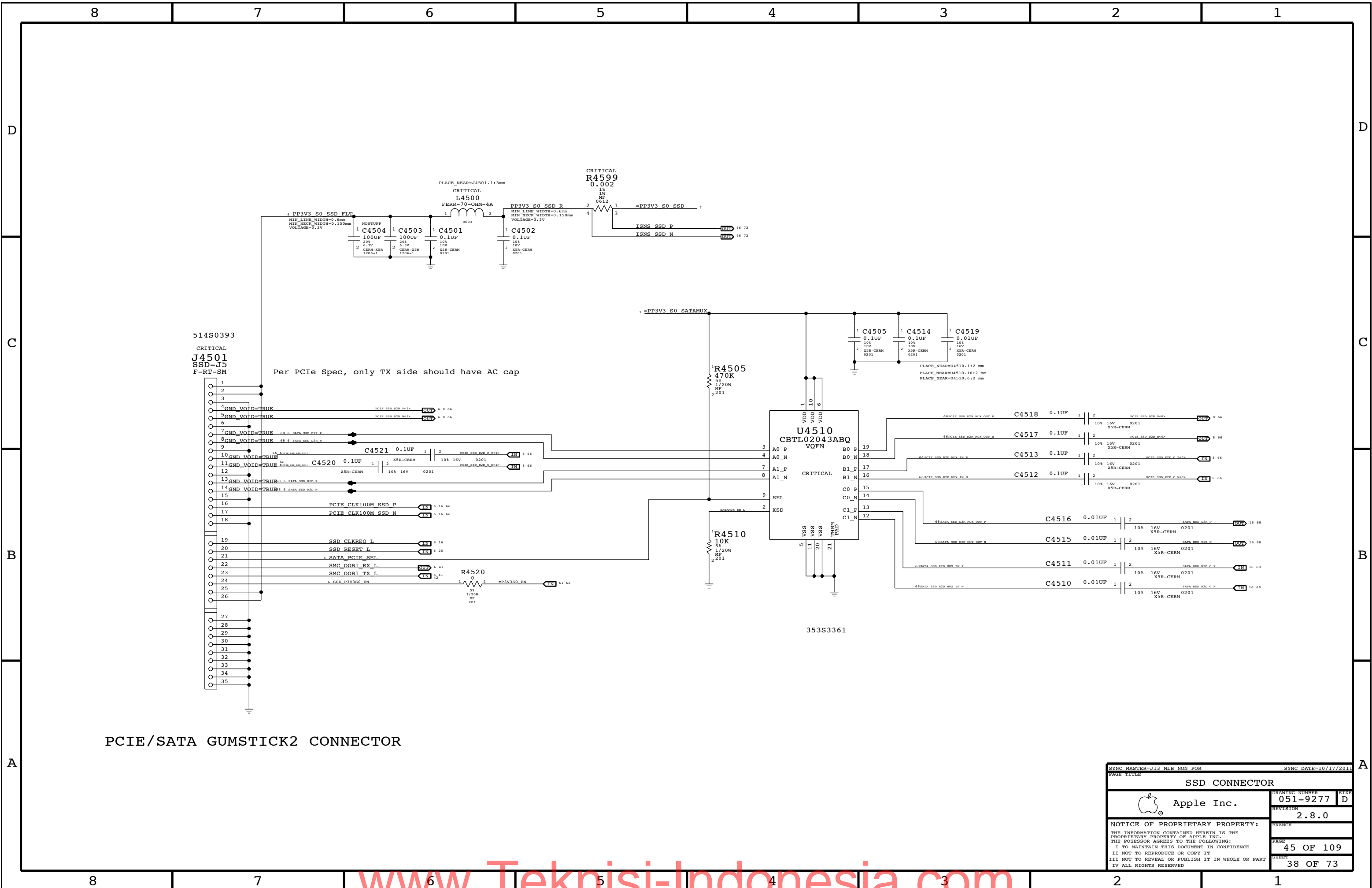


## 1.05V TBT "CIO" Switch




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TBT Power Support		051-9277	
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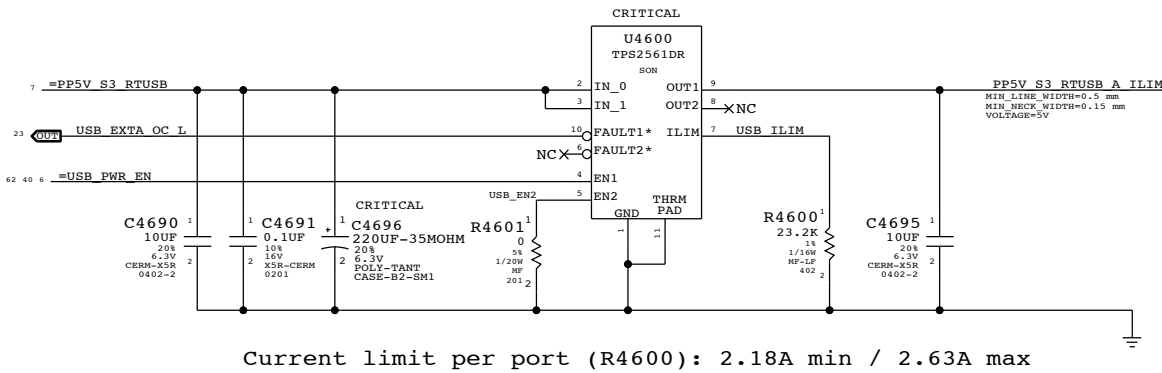


PCIE/SATA GUMSTICK2 CONNECTOR

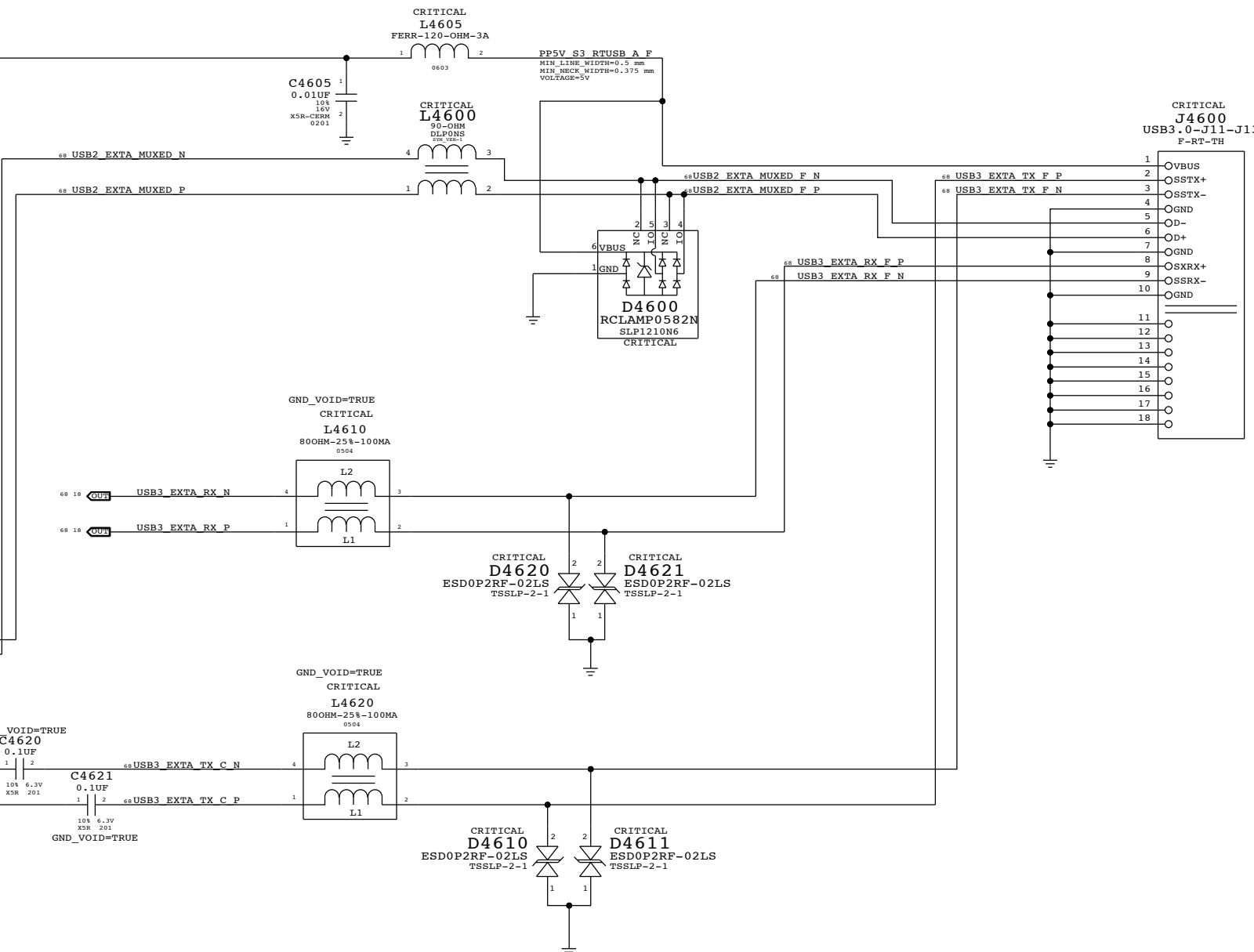
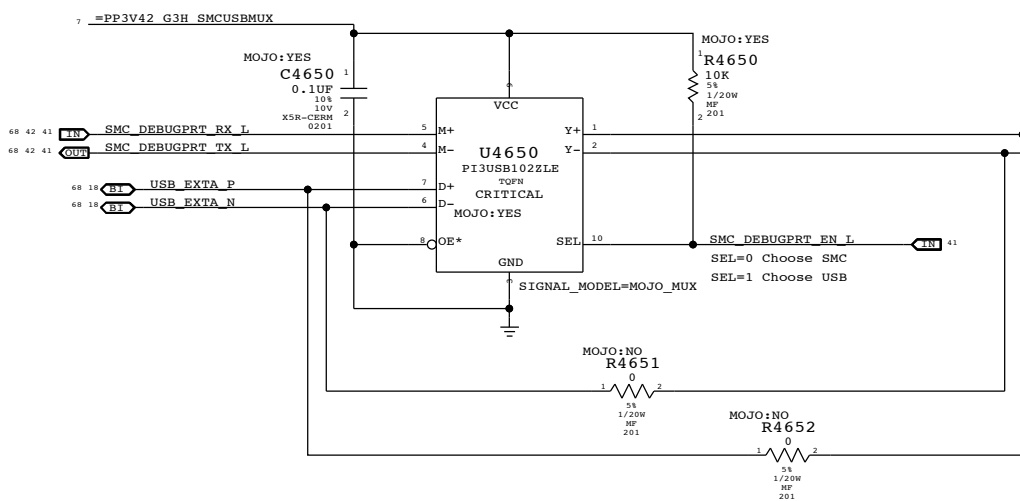
SYNC MASTER=J13 MLB NON POR		SYNC DATE=10/17/2011	
PAGE TITLE			
SSD CONNECTOR			
 Apple Inc.	DRAWING NUMBER	051-9277	SIZE D
	REVISION	2.8.0	
	BRANCH		
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		SHEET	38 OF 73


Right USB Port A

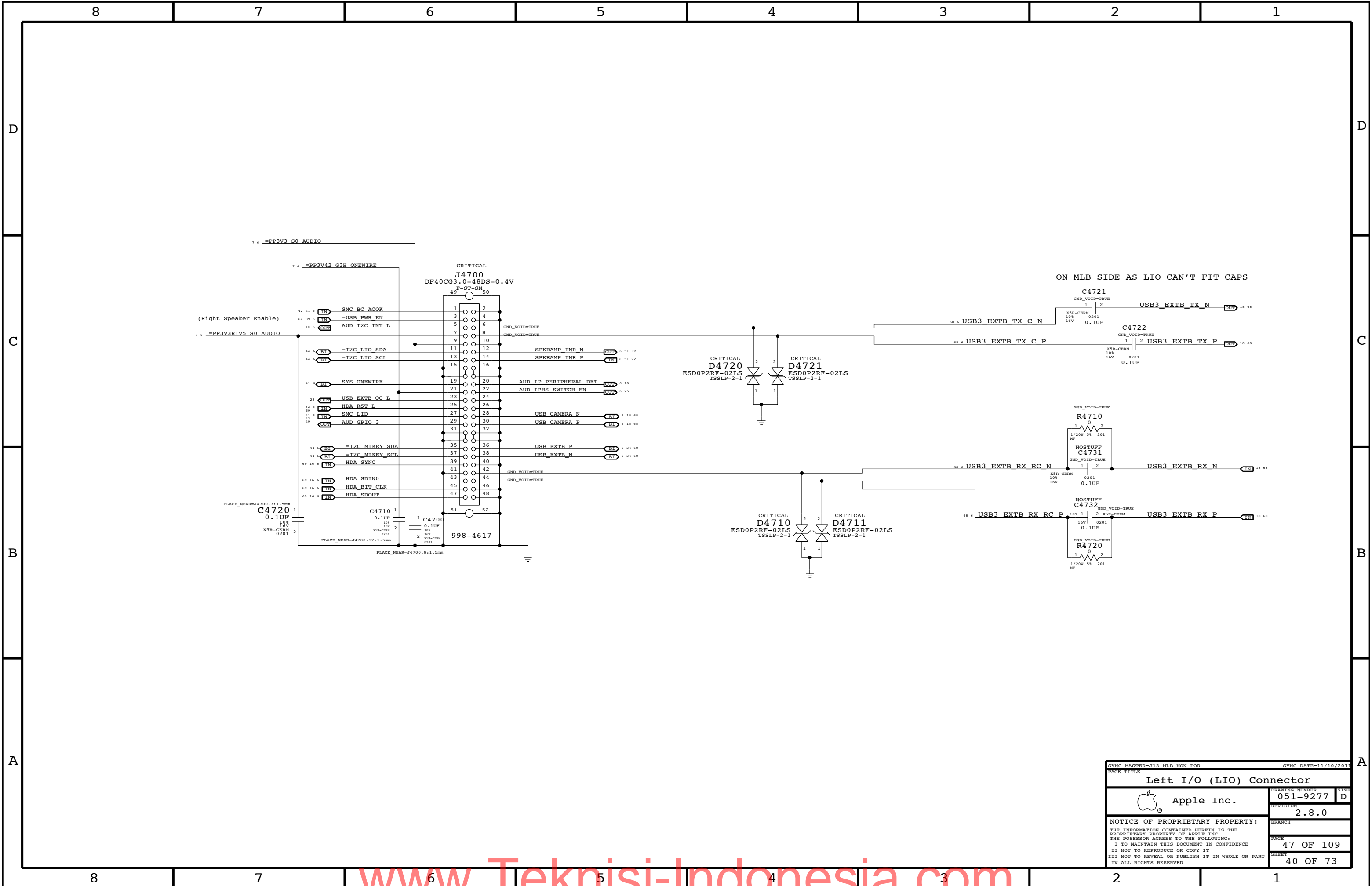
USB Port Power Switch



Mojo SMC Debug Mux



SYNC MASTER=J11 MLB		SYNC DATE=09/30/2011	
PAGE TITLE			
External A USB3 Connector			
 Apple Inc.		DRAWING NUMBER	051-9277
		SIZE	D
		REVISION	2.8.0
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		PAGE	46 OF 109
		SHEET	39 OF 73





8	7	6	5	4	3	2	1
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## C



## A

8	7	6	5	4	3	2	1
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MP-LP  
402

8 7 6 5 4 3

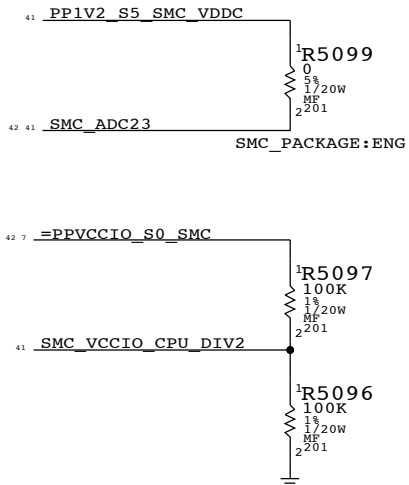
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```

41  SMC_DP_HPD_L           = NC_SMC_DP_HPD_L
53 55  =CHGR_ACOK           = SMC_BC_ACOK           6 40 41 42
41  HSIDE_ISENSE_OC       = NC_HSIDE_ISENSE_OC
41  SMBUS_SMC_4_ASF_SCL   = NC_SMBUS_SMC_4_ASF_SCL
41  SMBUS_SMC_4_ASF_SDA   = NC_SMBUS_SMC_4_ASF_SDA
41  BDV_BKL_PWM           = NC_BDV_BKL_PWM
42  SMC_PME_S4_DARK_L     = NC_PDCON_STATE_CHANGE_SMC_33
41  MAKE_BASE=TRUE
41  SMC_T25_EN_L          = NC_SMC_T25_EN_L
41  MAKE_BASE=TRUE

```

Figure 10: Schematic of the SPI peripheral connections. The diagram shows four SPI peripheral connections (R5021, R5022, R5023, R5024) connected to the SPI\_SMC\_MISO, SPI\_SMC\_MOSI, SPI\_SMC\_CLK, and SPI\_SMC\_CS\_L pins. Each connection is labeled with a resistor value (15 ohms) and a capacitor value (1/20W MF 201). The connections are also labeled with the SPI peripheral name (SPI\_MLB\_MISO, SPI\_MLB\_MOSI, SPI\_MLB\_CLK, SPI\_MLB\_CS\_L) and the location (PLACE\_NEAR=U6100.2:1MM).



7 =PP3V3\_S5\_SMCBATLOW

41 37

R5040<sup>1</sup>  
100K  
5%  
1/20W  
MF  
2012

CRITICAL  
Q5040  
SSM3K15AMFVAPE

VESM

PM\_BATLOW\_L

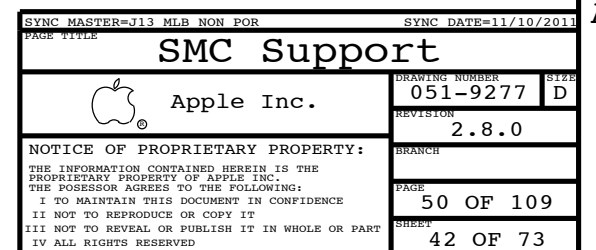
64 1 MAIN

17 SUP

R5041<sup>0</sup>  
20K  
5%  
1/16W  
MF-1F  
402

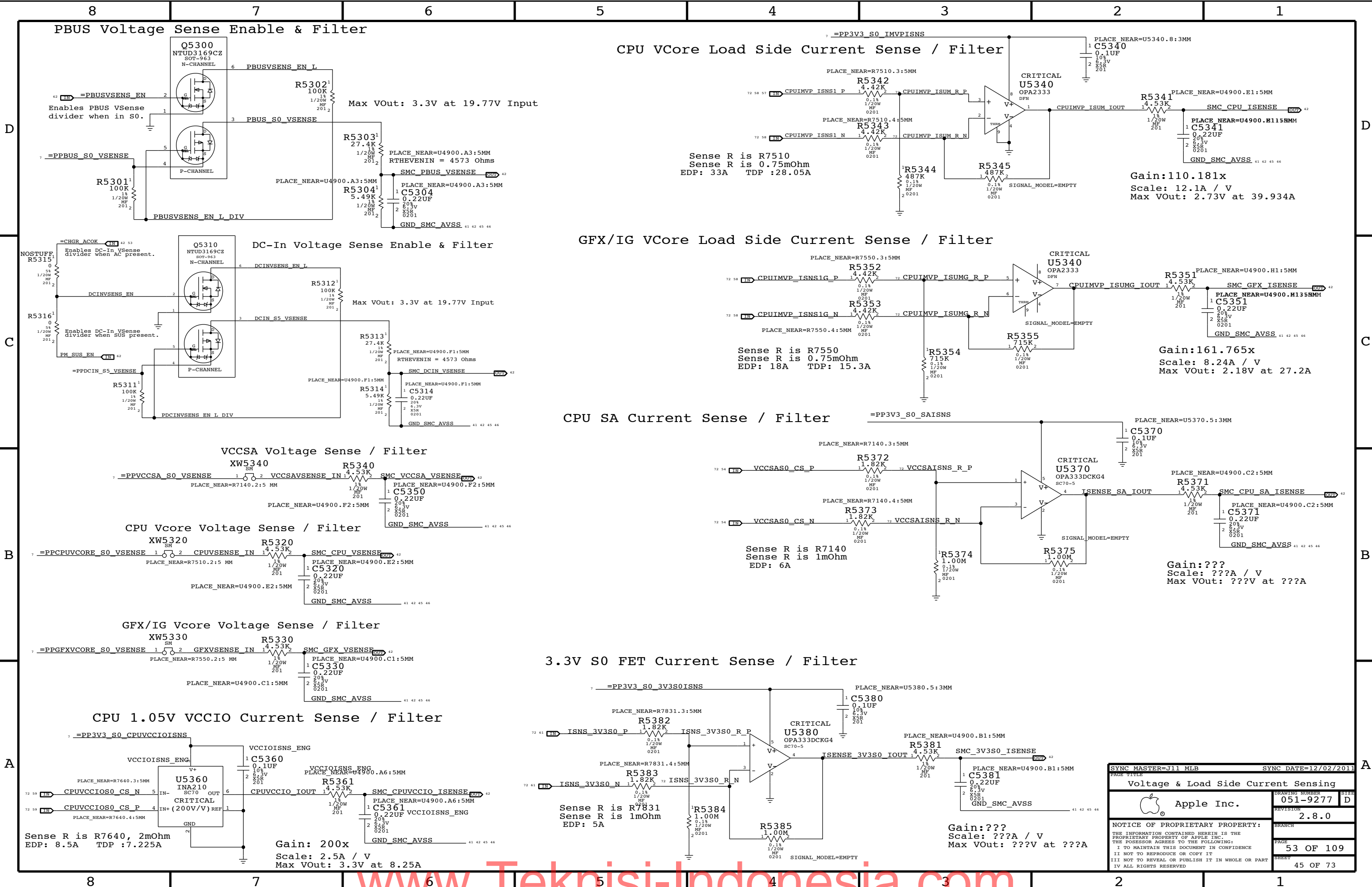
NOSTUFF

Internal 20K pull-up on PM\_BATLOW\_L in PCH.

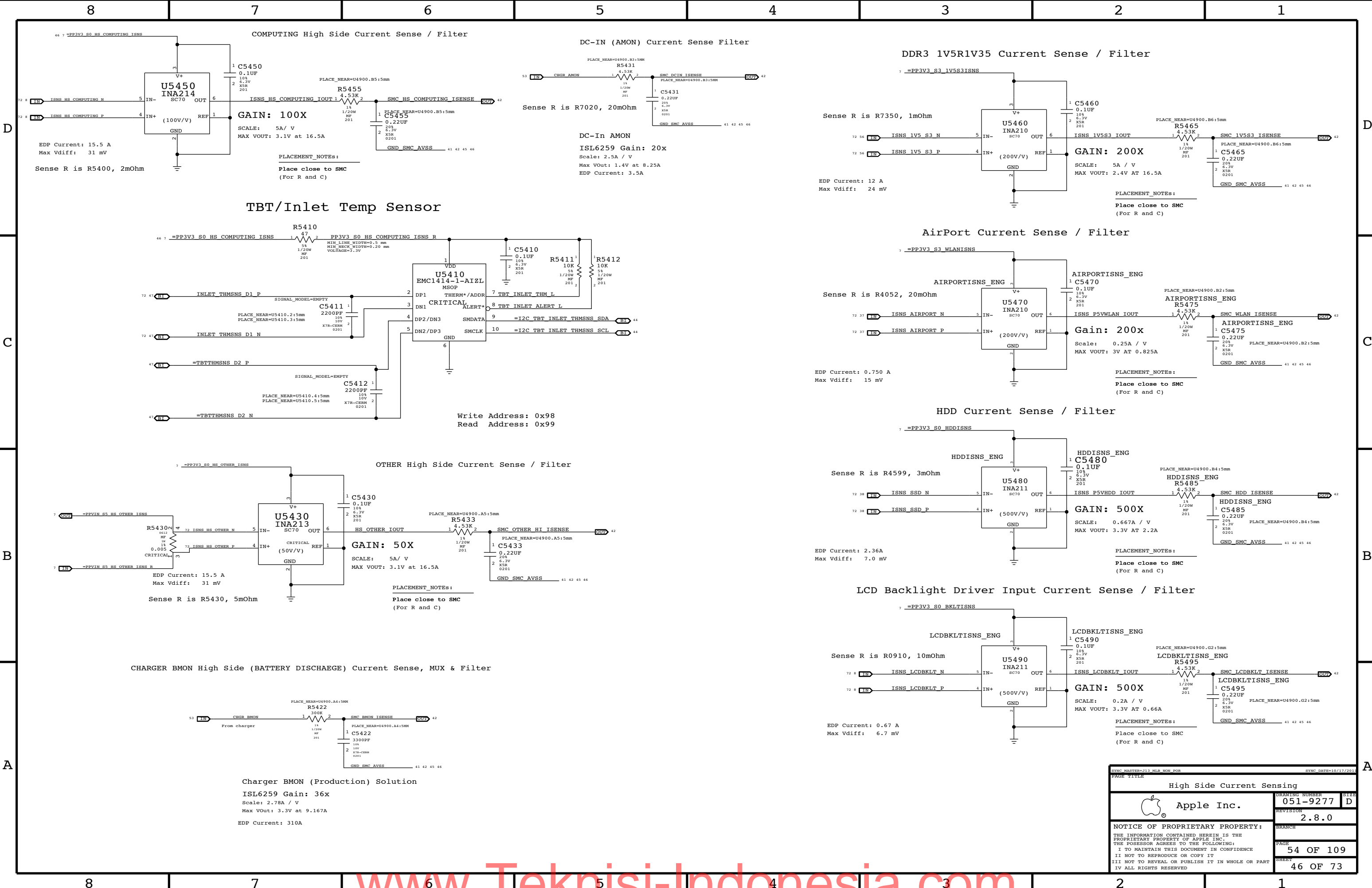
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SYNC MASTER=J11 MLB		SYNC DATE=12/02/2011	
PAGE TITLE		DRAWING NUMBER	
Voltage & Load Side Current Sensing		051-9277	
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CPU Proximity Sensor

TBT Die

Replacing caps with 100K PD on ISENSE SMC inputs

TBT,MLB Bottom & Inlet Proximity Sensors

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,NP,1/20W,100K OHM,5,0201,SMD	C5361		VCCIOISNS_PROD
117S0008	1	RES,NP,1/20W,100K OHM,5,0201,SMD	C5475		AIRPORTISNS_PROD
117S0008	1	RES,NP,1/20W,100K OHM,5,0201,SMD	C5485		HDDISNS_PROD
117S0008	1	RES,NP,1/20W,100K OHM,5,0201,SMD	C5495		LCDBKLTISNS_PROD

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CPU Proximity Sensor

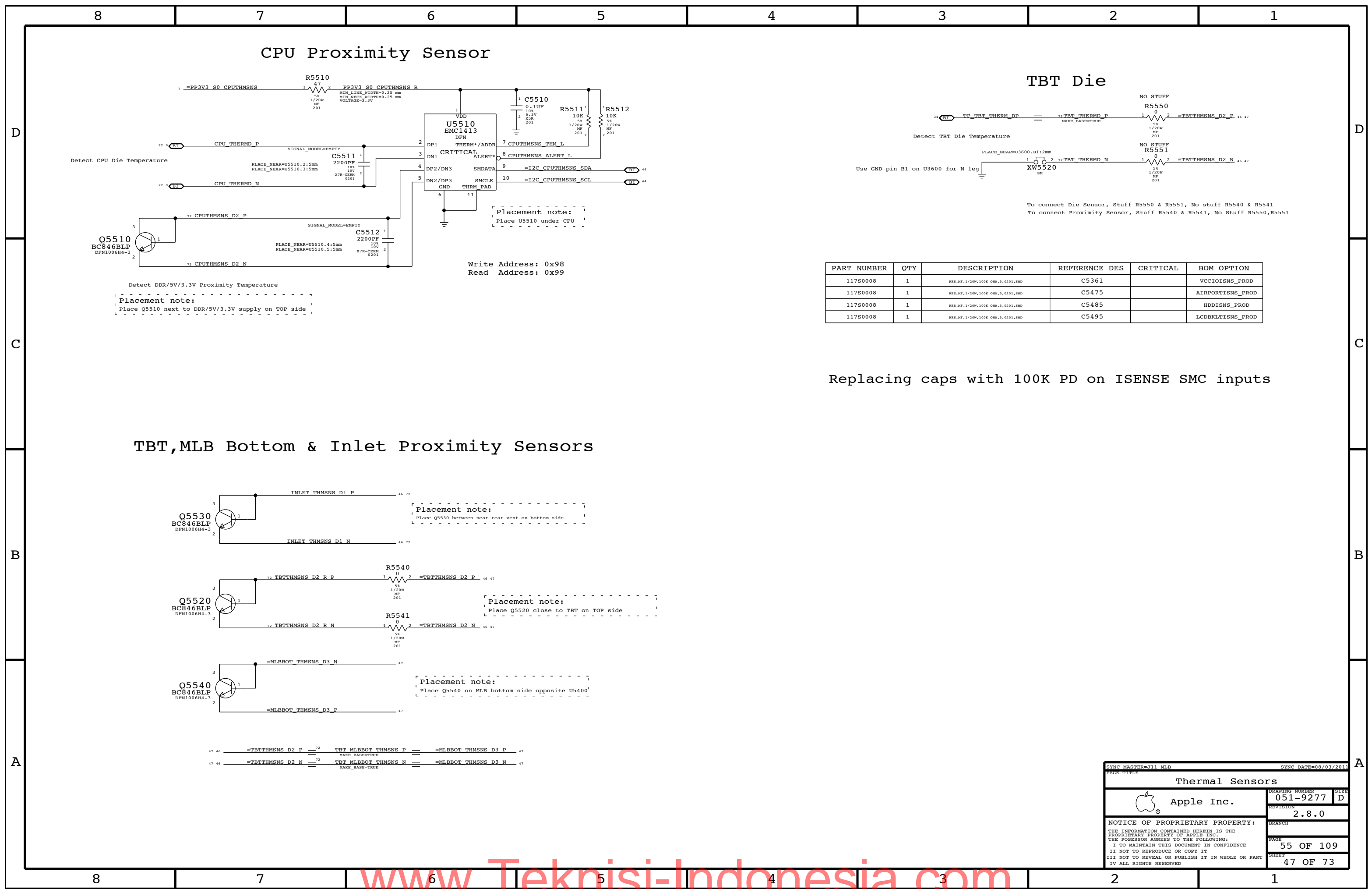
TBT Die

Replacing caps with 100K PD on ISENSE SMC inputs

TBT,MLB Bottom & Inlet Proximity Sensors

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	1	RES,NP,1/20W,100K OHM,5,0201,SMD	C5361		VCCIOISNS_PROD
117S0008	1	RES,NP,1/20W,100K OHM,5,0201,SMD	C5475		AIRPORTISNS_PROD
117S0008	1	RES,NP,1/20W,100K OHM,5,0201,SMD	C5485		HDDISNS_PROD
117S0008	1	RES,NP,1/20W,100K OHM,5,0201,SMD	C5495		LCDBKLTISNS_PROD

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CPU Proximity Sensor

Detect CPU Die Temperature

Detect DDR/5V/3.3V Proximity Temperature

Placement note:  
Place U5510 under CPU

Write Address: 0x98  
Read Address: 0x99

TBT Die

Detect TBT Die Temperature

Use GND pin B1 on U3600 for N leg

To connect Die Sensor, Stuff R5550 & R5551, No stuff R5540 & R5541  
To connect Proximity Sensor, Stuff R5540 & R5541, No Stuff R5550,R5551

Replacing caps with 100K PD on ISENSE SMC inputs

TBT,MLB Bottom & Inlet Proximity Sensors

Placement note:  
Place Q5530 between rear vent on bottom side

Placement note:  
Place Q5520 close to TBT on TOP side

Placement note:  
Place Q5540 on MLB bottom side opposite U5400

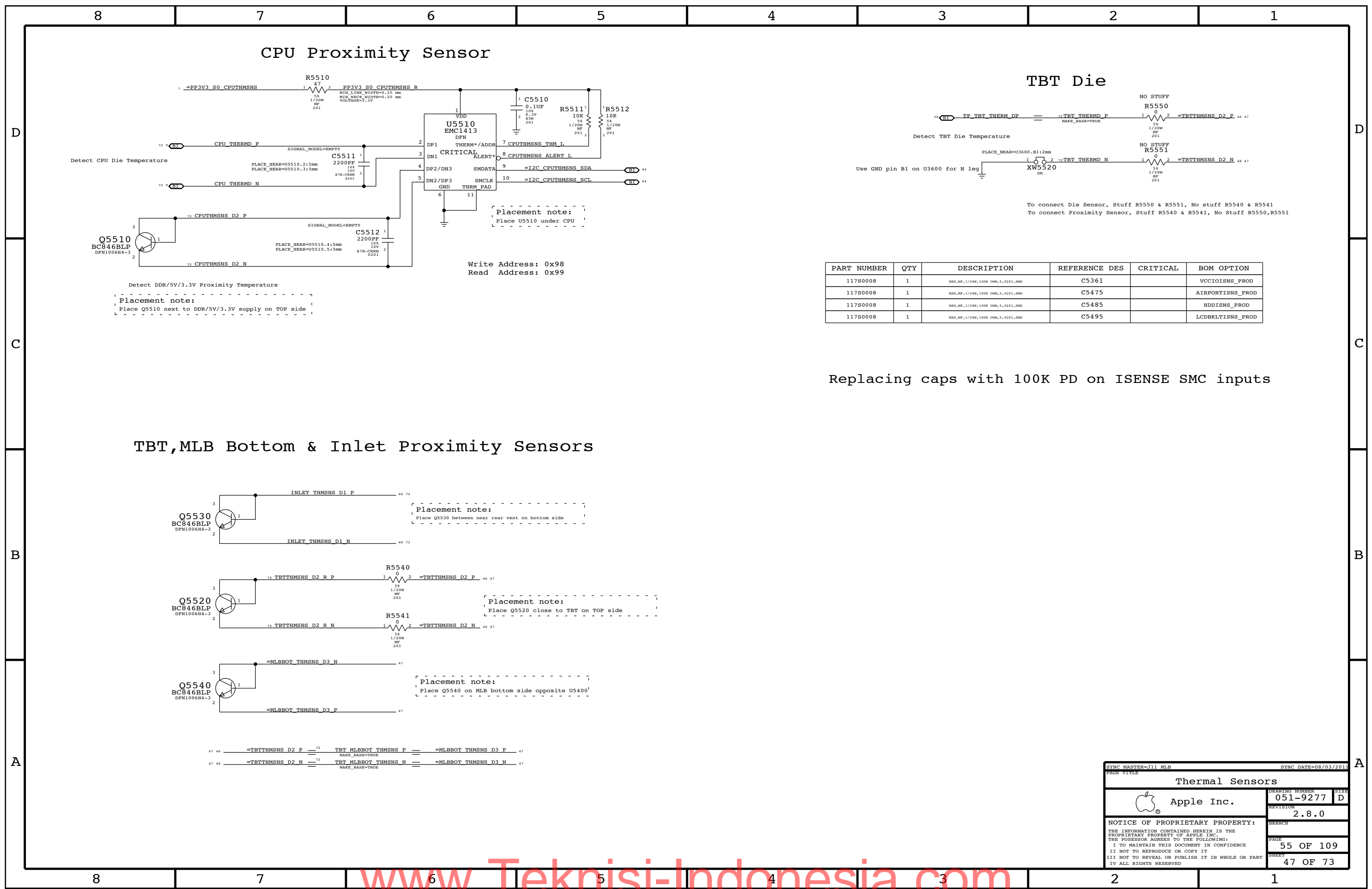
Thermal Sensors

Apple Inc.

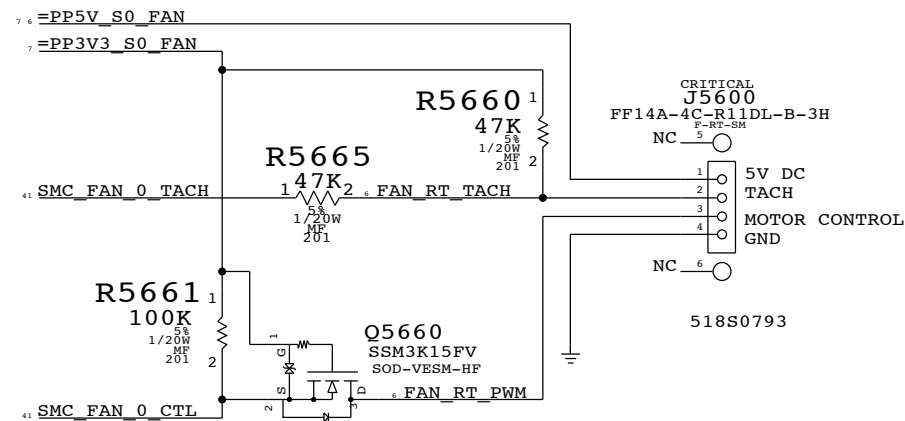
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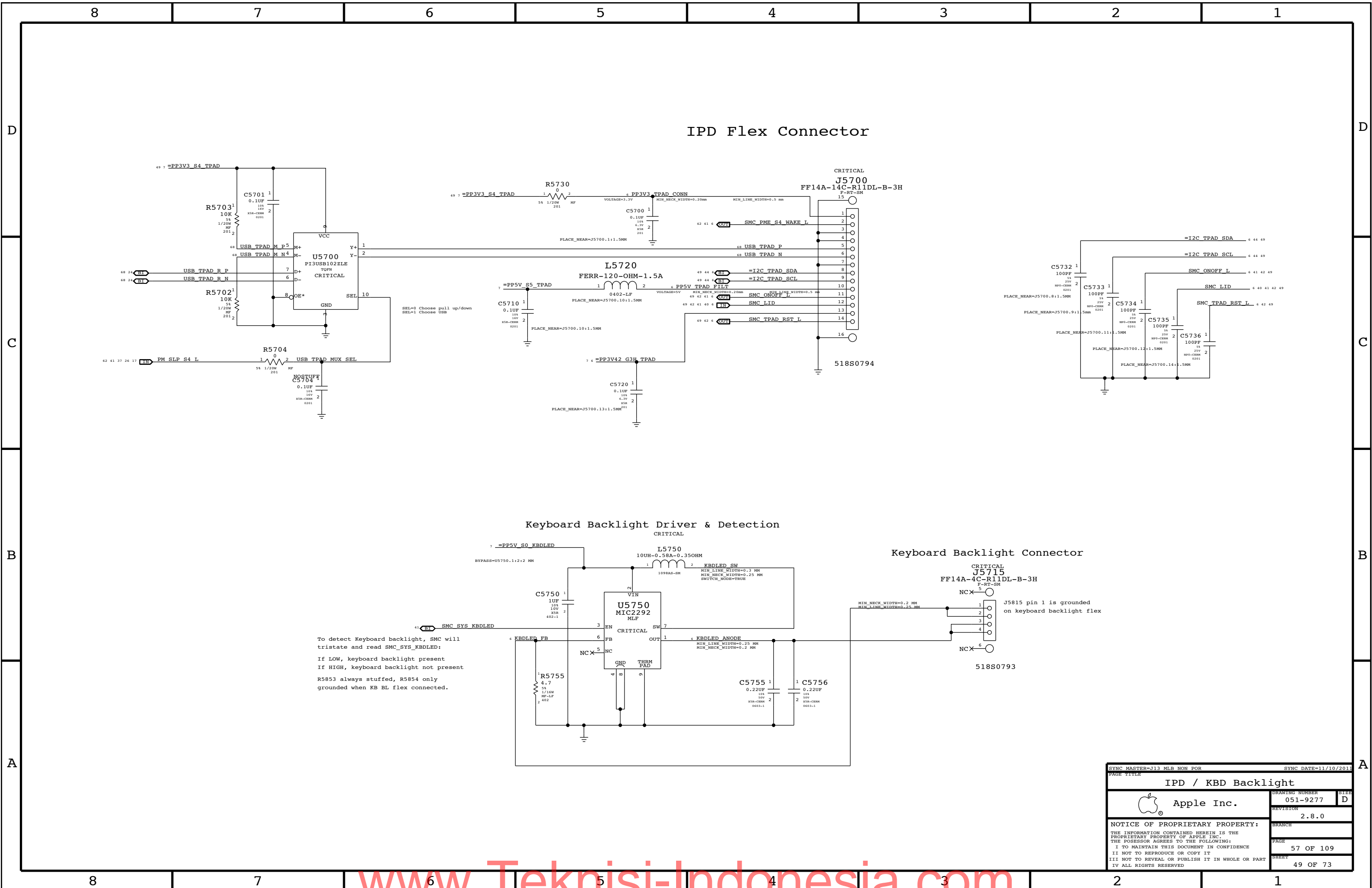
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051-9277  
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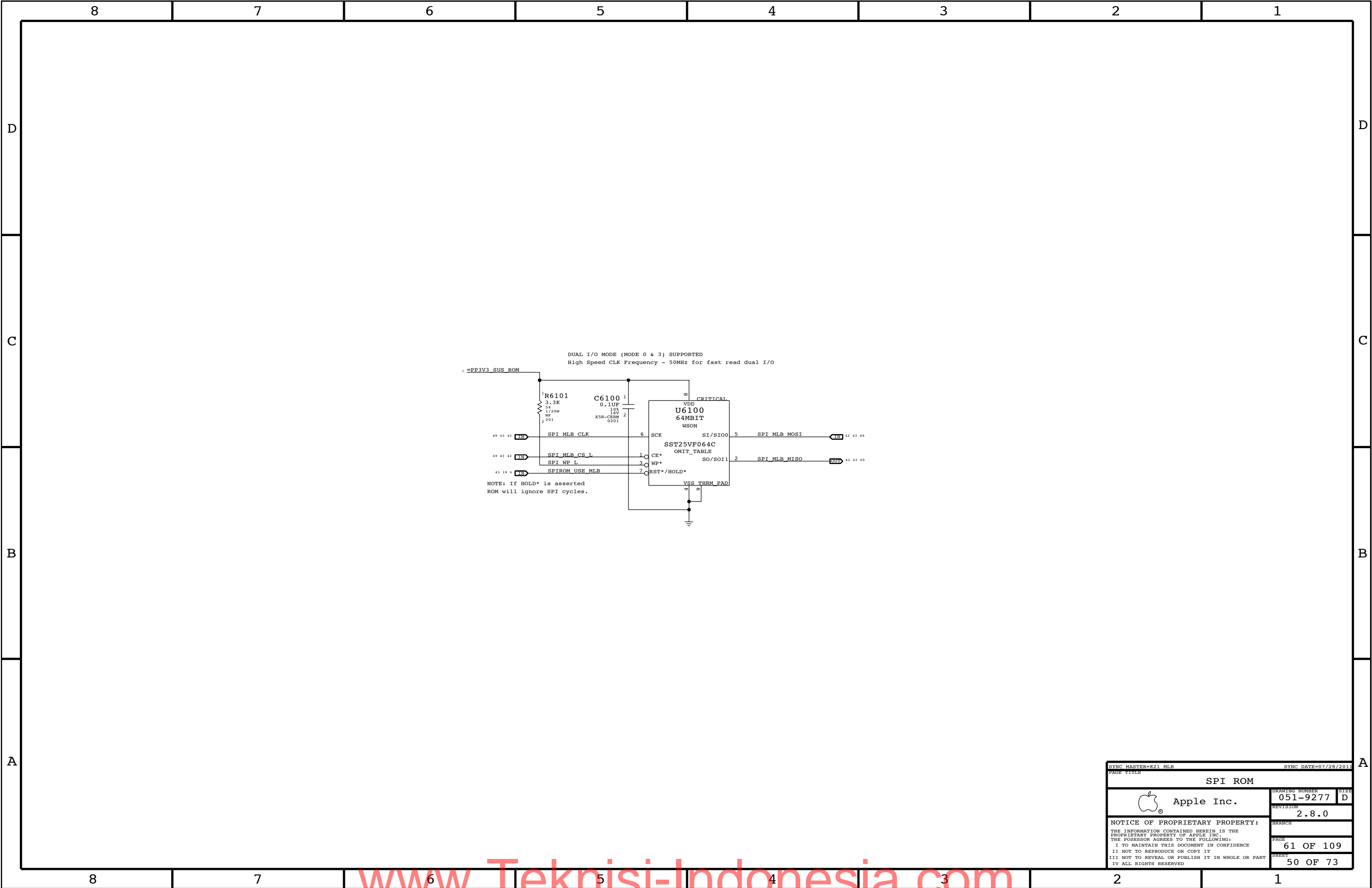
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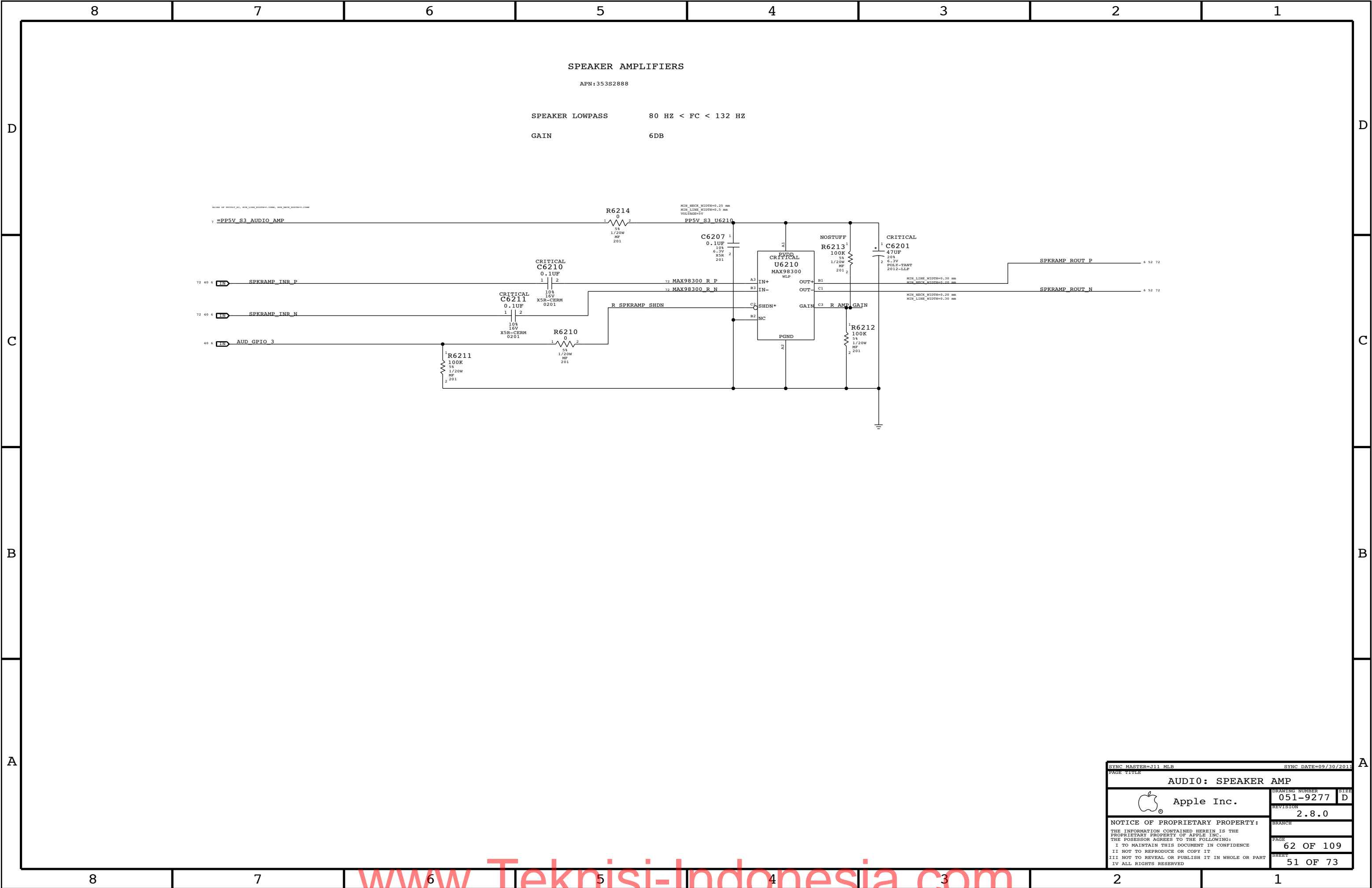
# FAN CONNECTOR



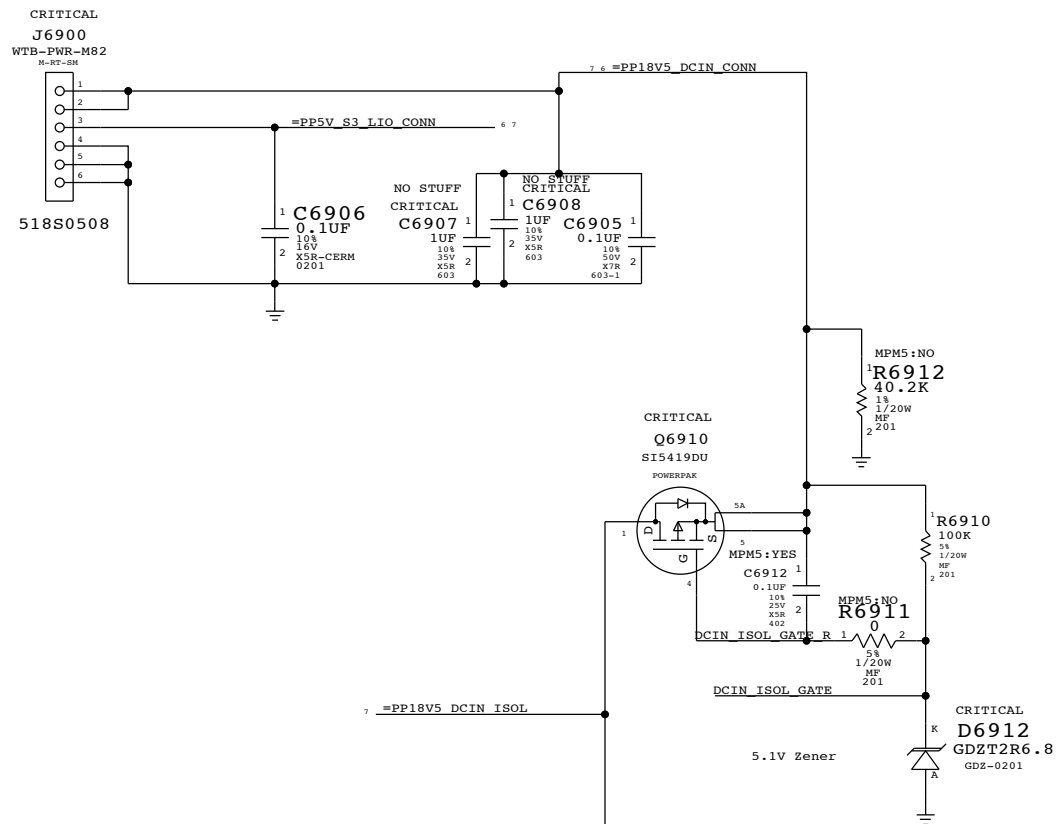
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DRAWING NUMBER		051-9277	SIZE D
REVISION		2.8.0	BRANCH
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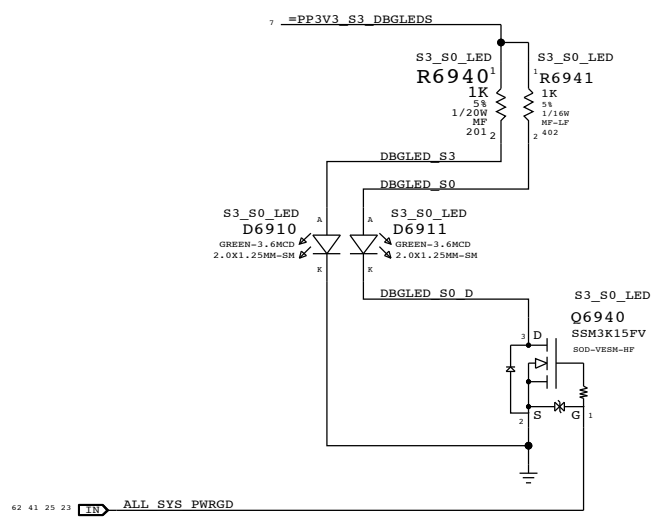


MLB to LIO Power Cable Connector

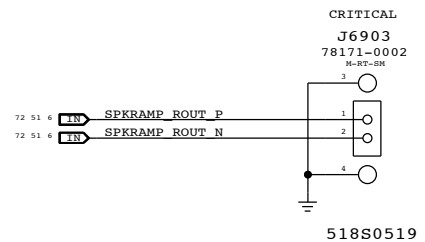


Debug LEDs

(For development only)



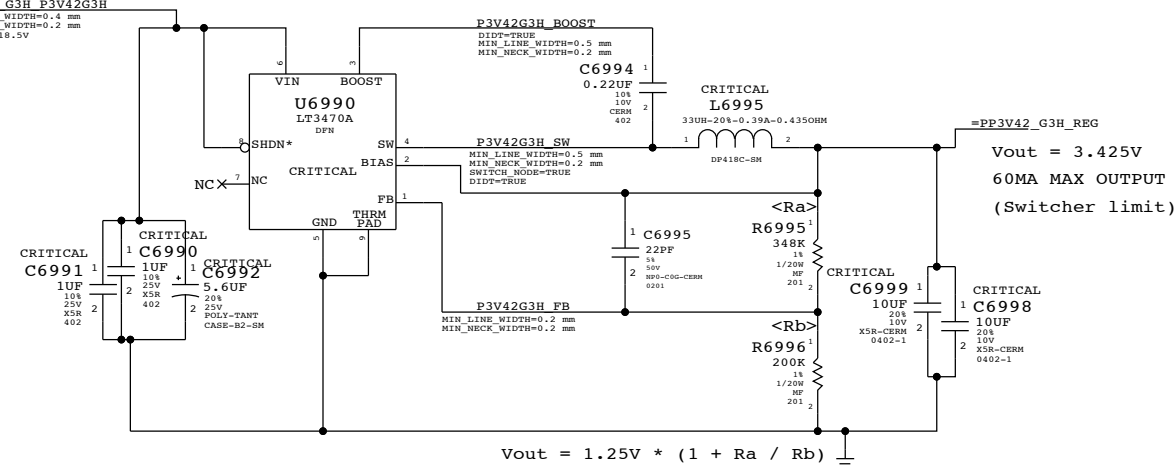
Right Speaker Connector



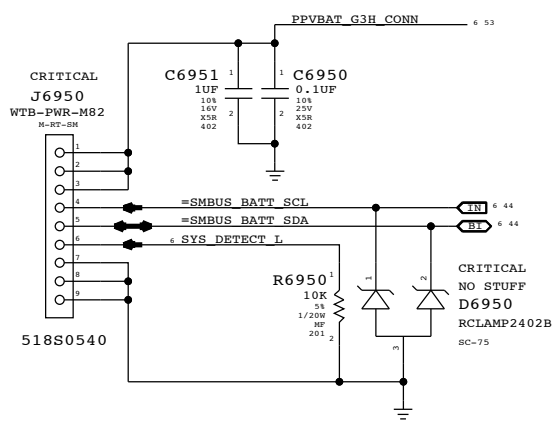
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118S0560	1	RES,RP,1/20W,50.90OHM,1,0201,SMD	R6912		MPM5:YES
117S0008	1	RES,RP,1/20W,1000OHM,1,0201,SMD	R6911		MPM5:YES

3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC Vref generator



K16-Specific Battery Connector



D

C

B

A

D

C

B

A

DC-In & Battery Connectors

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051-9277

2.8.0

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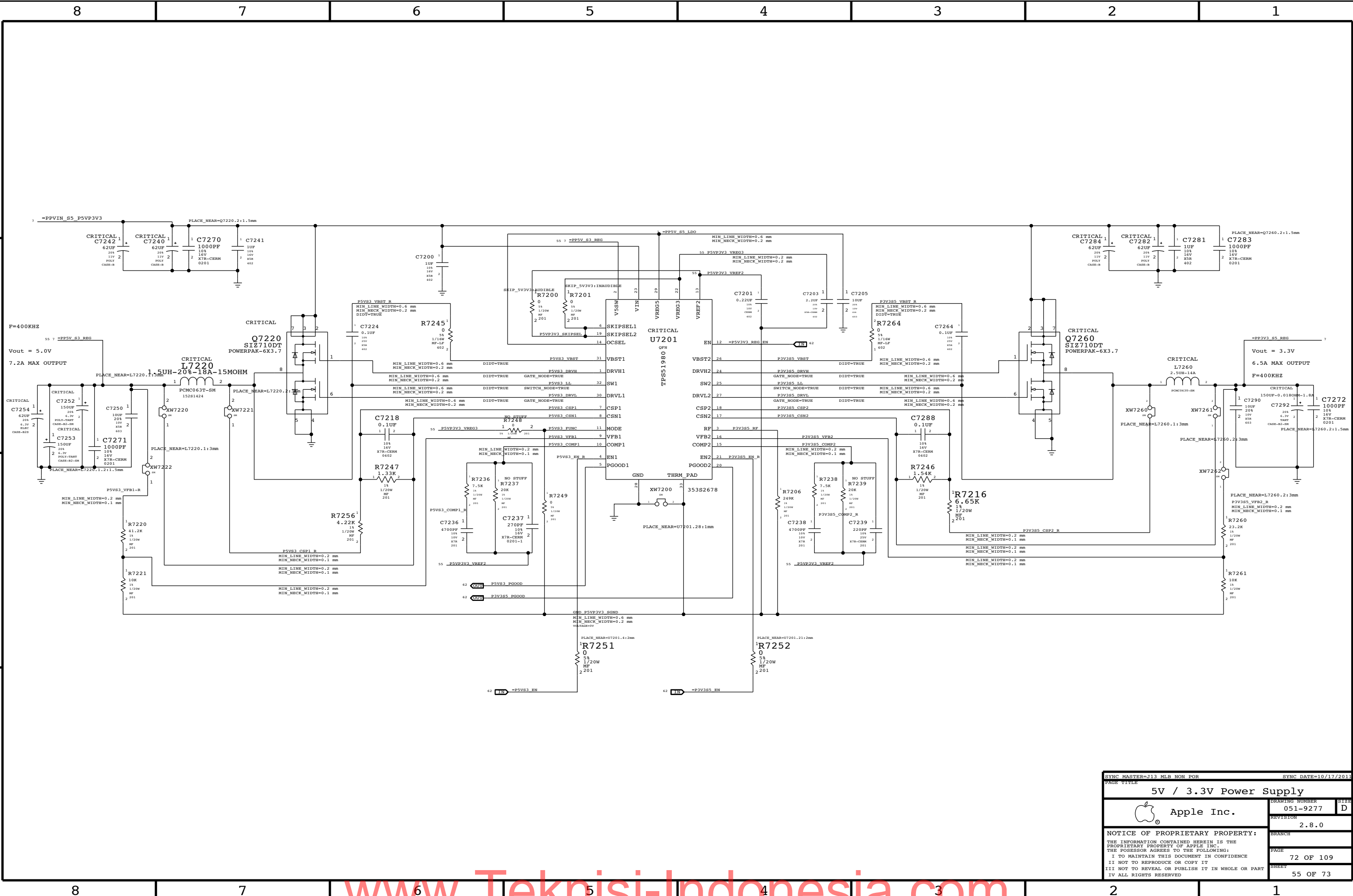
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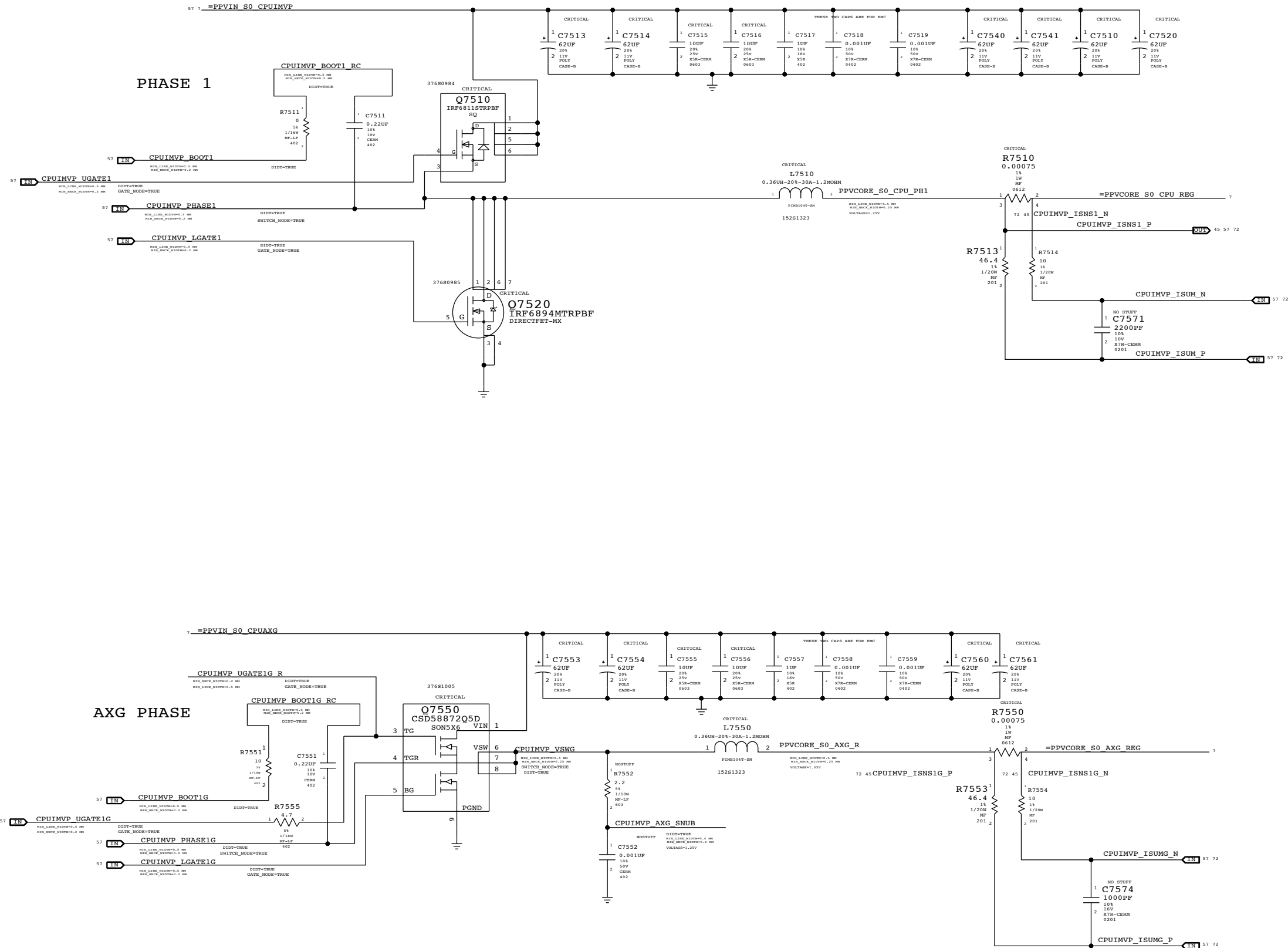


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PAGE TITLE			
5V / 3.3V Power Supply			
 Apple Inc.	DRAWING NUMBER	051-9277	SIZE D
	REVISION	2.8.0	
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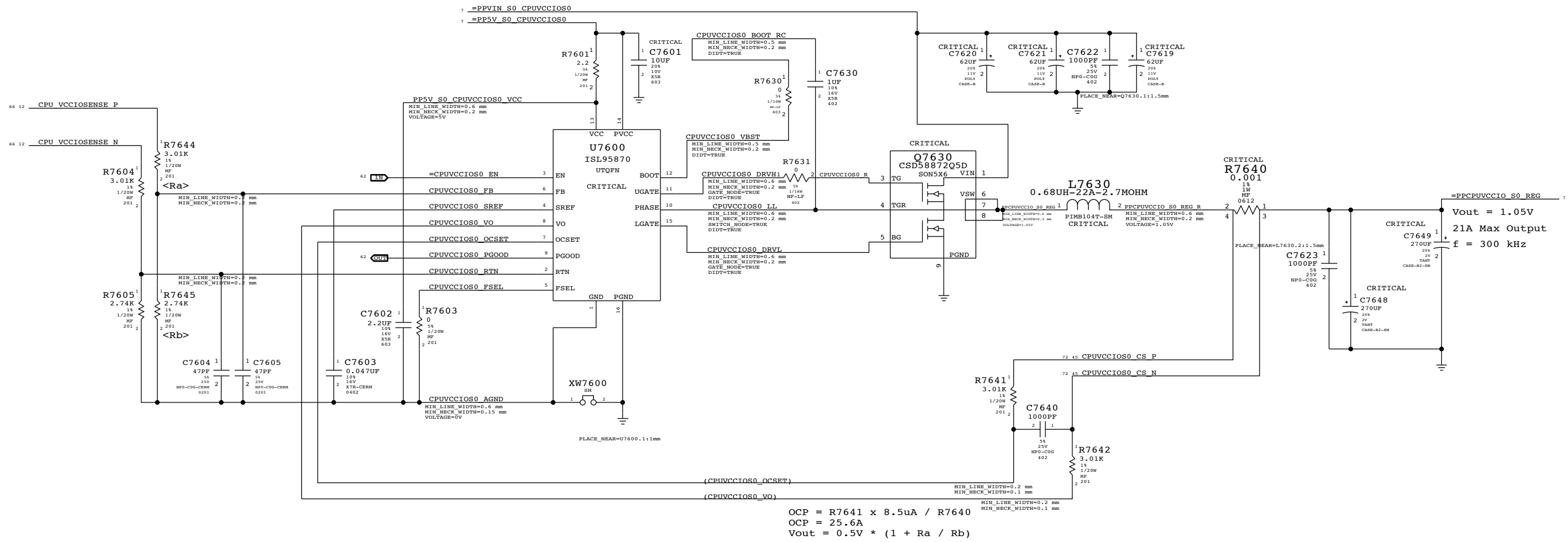


# CPU=IV Bridge ULV, AXG=GT2



CPU IMVP7 & AXG VCore Output		
Apple Inc.	DRAWING NUMBER	051-9277
	REVISION	2.8.0
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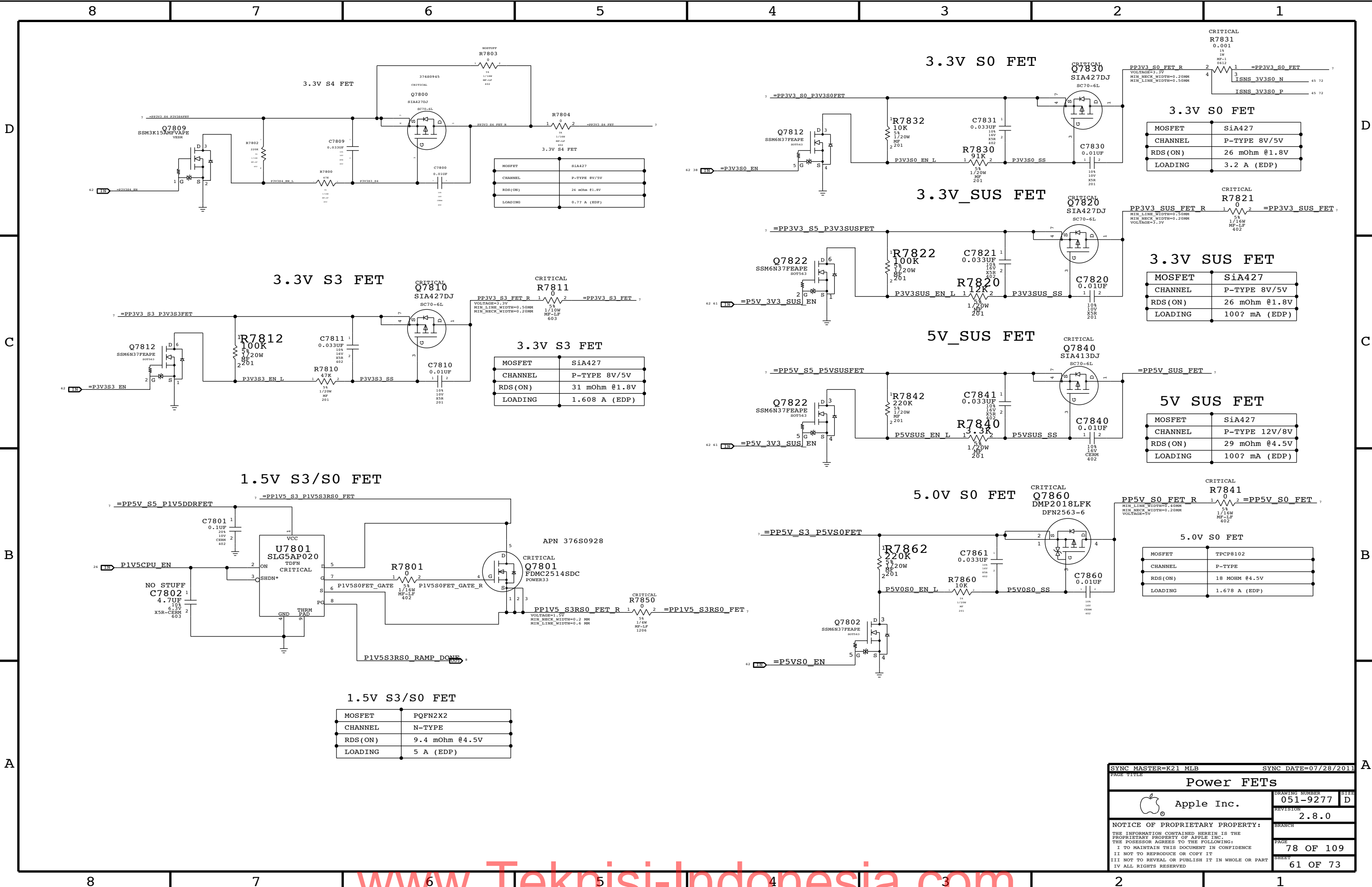
CPU VCCIO (1.05V S0) Regulator



OCF = R7641 x 8.5uA / R7640  
OCF = 25.6A  
Vout = 0.5V \* (1 + Ra / Rb)

CPU VCCIO (1.05V) Power Supply	
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SYNC DATE=07/28/2011

Power FETs

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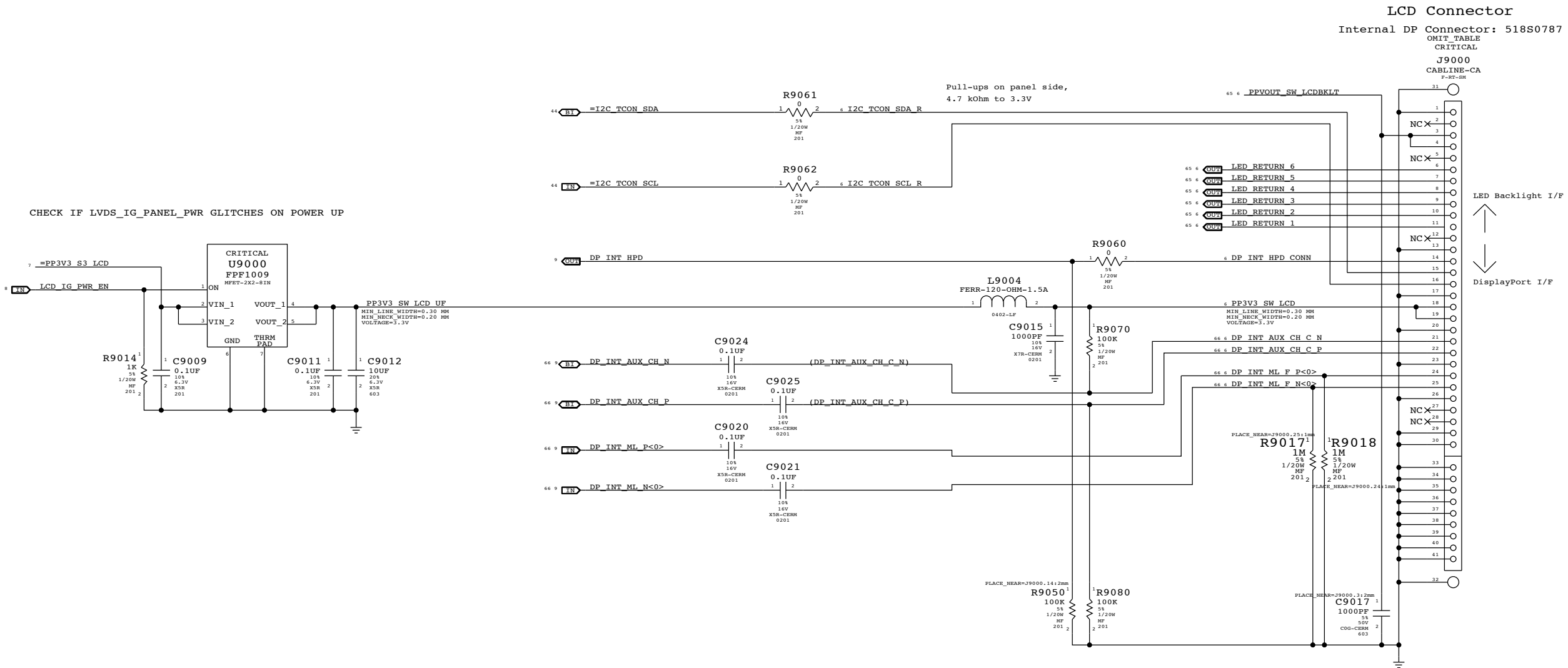
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
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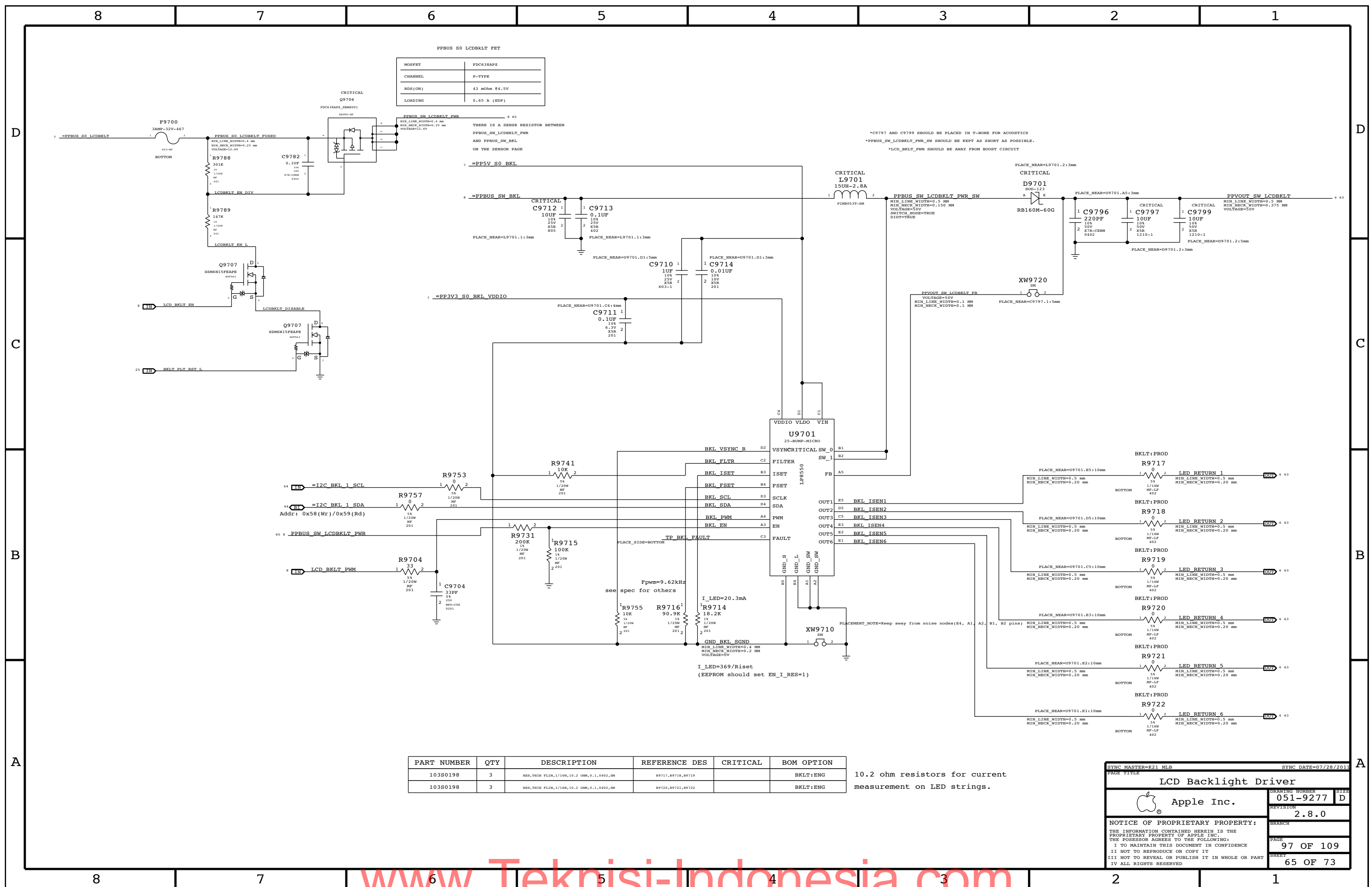
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
518S0829	1	CONN212-AK,P=0.4,10P,W=BOSS,HP	J9000		



SYNC MASTER=K21 MLB		SYNC DATE=07/28/2011	
PAGE TITLE			
Internal DisplayPort Connector		DRAWING NUMBER	
 Apple Inc.		DRAWING NUMBER	051-9277
		SIZE	D
		REVISION	2.8.0
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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	0.100 MM	0.100 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_AGTL	*	=STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_8MIL	*	*	CPU_8MIL_2ANY

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_ITP	*	*	CPU_ITP_2ANY

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	CPU_COMP	*	CPU_COMP_2SELF
CPU_COMP	*	*	CPU_COMP_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_COMP_2SELF	TOP,BOTTOM	=6x_DIELECTRIC	?
CPU_COMP_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_VCCSENSE	CPU_VCCSENSE	*	CPU_VCCSENSE_2SELF
CPU_VCCSENSE	*	*	CPU_VCCSENSE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_VCCSENSE_2SELF	*	=4x_DIELECTRIC	?
CPU_VCCSENSE_2OTHER	*	=6x_DIELECTRIC	?

PCI-Express Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
CLK_PCIE_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

PCIe Clock Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	CLK_PCIE	*	CLK_PCIE_2SELF
CLK_PCIE	*	*	CLK_PCIE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_PCIE_2SELF	*	=4x_DIELECTRIC	?
CLK_PCIE_2OTHER	*	=6x_DIELECTRIC	?

CPU PCIe Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_CPU_TX	PCIE_CPU_TX	*	PCIE_TX2TX
PCIE_CPU_RX	PCIE_CPU_RX	*	PCIE_RX2RX
PCIE_CPU_TX	*_CPU_TX	*	PCIE_TX2OTHERTX
PCIE_CPU_RX	*_CPU_RX	*	PCIE_RX2OTHERRX
PCIE_CPU_TX	*_CPU_TX	*	PCIE_TX2RX
PCIE_CPU_RX	*_CPU_TX	*	PCIE_RX2TX
PCIE_CPU_TX	*_TX	*	PCIE_2OTHERHS
PCIE_CPU_RX	*_TX	*	PCIE_2OTHERHS
PCIE_CPU_TX	*_RX	*	PCIE_2OTHERHS
PCIE_CPU_RX	*_RX	*	PCIE_2OTHERHS
PCIE_CPU_TX	*	*	PCIE_2OTHER
PCIE_CPU_RX	*	*	PCIE_2OTHER

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_TX2TX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_RX2RX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_TX2OTHERTX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_RX2OTHERRX	TOP,BOTTOM	=5x_DIELECTRIC	?
PCIE_TX2RX	TOP,BOTTOM	=7x_DIELECTRIC	?
PCIE_RX2TX	TOP,BOTTOM	=7x_DIELECTRIC	?
PCIE_2OTHERHS	TOP,BOTTOM	=6x_DIELECTRIC	?
PCIE_2OTHER	TOP,BOTTOM	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_TX2TX	*	=2.5x_DIELECTRIC	?
PCIE_RX2RX	*	=2.5x_DIELECTRIC	?
PCIE_TX2OTHERTX	*	=4x_DIELECTRIC	?
PCIE_RX2OTHERRX	*	=4x_DIELECTRIC	?
PCIE_TX2RX	*	=6x_DIELECTRIC	?
PCIE_RX2TX	*	=6x_DIELECTRIC	?
PCIE_2OTHERHS	*	=4x_DIELECTRIC	?
PCIE_2OTHER	*	=3x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_PCH_TX	PCIE_PCH_TX	*	PCIE_TX2TX
PCIE_PCH_RX	PCIE_PCH_RX	*	PCIE_RX2RX
PCIE_PCH_TX	*_PCH_TX	*	PCIE_TX2OTHERTX
PCIE_PCH_RX	*_PCH_RX	*	PCIE_RX2OTHERRX
PCIE_PCH_TX	*_PCH_RX	*	PCIE_TX2RX
PCIE_PCH_RX	*_PCH_TX	*	PCIE_RX2TX
PCIE_PCH_TX	*_TX	*	PCIE_2OTHERHS
PCIE_PCH_RX	*_TX	*	PCIE_2OTHERHS
PCIE_PCH_TX	*_RX	*	PCIE_2OTHERHS
PCIE_PCH_RX	*_RX	*	PCIE_2OTHERHS
PCIE_PCH_TX	*	*	PCIE_2OTHER
PCIE_PCH_RX	*	*	PCIE_2OTHER

SOURCE: 471984\_Chief\_River\_MS\_PDG\_1.0 and the spacing rule is adjusted per SI team feedback.

CPU Net Properties

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
DMI_S2N	PCIE_80D	PCIE_PCH_TX	DMI_S2N_P<3:0>
DMI_S2N	PCIE_80D	PCIE_PCH_TX	DMI_S2N_N<3:0>
DMI_N2S	PCIE_80D	PCIE_PCH_RX	DMI_N2S_P<3:0>
DMI_N2S	PCIE_80D	PCIE_PCH_RX	DMI_N2S_N<3:0>
FDI_DATA	PCIE_80D	PCIE_PCH_RX	FDI_DATA_P<7:0>
FDI_DATA	PCIE_80D	PCIE_PCH_RX	FDI_DATA_N<7:0>
CPU_45S	CPU_45S	CPU_AGTL	FDI_FSYNC<1..0>
CPU_45S	CPU_AGTL	CPU_AGTL	FDI_LSYNC<1..0>
CPU_45S	CPU_AGTL	CPU_AGTL	FDI_INT
CPU_PECT	CPU_45S	CPU_COMP	CPU_PECT
PM_SYNC	CPU_45S	CPU_AGTL	PM_SYNC
PM_MEM_PWRGD	CPU_45S	CPU_AGTL	PM_MEM_PWRGD
CPU_45S	CPU_ITP	CPU_ITP	XDP_DBRESET_L
CPU_45S	CPU_ITP	CPU_ITP	XDP_CPU_RDY_L
CPU_45S	CPU_ITP	CPU_ITP	XDP_CPU_PREQ_L
CPU_27P4S	CPU_COMP	CPU_COMP	EDP_COMP
CPU_27P4S	CPU_COMP	CPU_COMP	CPU_PEG_COMP
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<0>
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<1>
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2>
CPU_45S	CPU_ITP	CPU_ITP	CPU_CFG<11..0>
CPU_CATERR_L	CPU_45S	CPU_AGTL	CPU_CATERR_L
CPU_VCCIO_SEL	CPU_45S	CPU_AGTL	CPU_VCCIO_SEL
CPU_PROCHOT_L	CPU_45S	CPU_AGTL	CPU_PROCHOT_L
CPU_PWRGD	CPU_45S	CPU_AGTL	CPU_PWRGD
PM_THRMTRIP_L	CPU_45S	CPU_8MIL	PM_THRMTRIP_L
DMI_CLK100M	CLK_PCIE_80D	CLK_PCIE	DMI_CLK100M_CPU_P
DMI_CLK100M	CLK_PCIE_80D	CLK_PCIE	DMI_CLK100M_CPU_N
DPLL_REF_CLK120M	CLK_PCIE_80D	CLK_PCIE	DPLL_REF_CLKP
DPLL_REF_CLK120M	CLK_PCIE_80D	CLK_PCIE	DPLL_REF_CLKN
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPCPU_CLK100M_P
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPCPU_CLK100M_N
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPXDP_CLK100M_P
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	ITPXDP_CLK100M_N
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	XDP_CPU_CLK100M_P
ITPCPU_CLK100M	CLK_PCIE_80D	CLK_PCIE	XDP_CPU_CLK100M_N
XDP_TDI	CPU_45S	CPU_ITP	XDP_CPU_TDI
XDP_TDO	CPU_45S	CPU_ITP	XDP_CPU_TDO
XDP_TMS	CPU_45S	CPU_ITP	XDP_CPU_TMS
XDP_TCK	CPU_45S	CPU_ITP	XDP_CPU_TCK
XDP_TRST_L	CPU_45S	CPU_ITP	XDP_CPU_TRST_L
XDP_BPM_L	CPU_45S	CPU_ITP	XDP_BPM_L<3..0>
(XDP_BPM_L_R_CFG)	CPU_45S	CPU_ITP	XDP_BPM_L<7..4>
(XDP_BPM_L_R_CFG)	CPU_45S	CPU_ITP	XDP_OBSDATA_B<3..0>
(FSB_CPURST_L)	CPU_45S	CPU_ITP	CPU_CFG<15..12>
CPU_VCCSENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_P
CPU_VCCSENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_VCCSENSE_N
CPU_VCCIOSENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_P
CPU_VCCIOSENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_VCCIOSENSE_N
CPU_AXG_SENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_P
CPU_AXG_SENSE	SENSE_1T01_P2MM	CPU_VCCSENSE	CPU_AXG_SENSE_N
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_P
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_N
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P
CPU_VALSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N
CPU_SVIDALERT_L	CPU_45S	CPU_COMP	CPU_VIDALERT_L
CPU_SVIDSClk	CPU_45S	CPU_COMP	CPU_VIDSClk
CPU_SVIDSOUT	CPU_45S	CPU_COMP	CPU_VIDSOUT
PCIE_CPU_MUX_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_P<0>
PCIE_CPU_MUX_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_C_N<0>
PCIE_CPU_MUX_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_MUX_IN_P
PCIE_CPU_MUX_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_MUX_IN_N
PCIE_CPU_MUX_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_P<0>
PCIE_CPU_MUX_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_N<0>
PCIE_CPU_MUX_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_MUX_OUT_P
PCIE_CPU_MUX_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_MUX_OUT_N
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_R2D_C_P<1>
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_R2D_C_N<1>
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_P<1>
PCIE_CPU_SSD_R2D	PCIE_80D	PCIE_CPU_TX	PCIE_SSD_R2D_N<1>
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_P<1>
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_N<1>
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_C_P<1>
PCIE_CPU_SSD_D2R	PCIE_80D	PCIE_CPU_RX	PCIE_SSD_D2R_C_N<1>
PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD_P
PCIE_CLK100M_SSD	CLK_PCIE_80D	CLK_PCIE	PCIE_CLK100M_SSD_N
DP_INT_ML	DP_80D	DP_TX	DP_INT_ML_P<3..0>
DP_INT_ML	DP_80D	DP_TX	DP_INT_ML_N<3..0>
DP_80D	DP_80D	DP_TX	DP_INT_ML_F_P<3..0>
DP_80D	DP_80D	DP_TX	DP_INT_ML_F_N<3..0>
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_C_P
DP_INT_AUXCH	DP_80D	DP_AUX	DP_INT_AUX_CH_C_N
DP_80D	DP_80D	DP_AUX	DP_INT_AUX_CH_P
DP_80D	DP_80D	DP_AUX	DP_INT_AUX_CH_N

Note: CPU\_8MIL and CPU\_ITP can be converted back to TABLE\_SPACING\_RULE once rdar://10308147 is resolved


Note: DisplayPort tables are on Page 103

SYNC MASTER=J13 CONSTRAINTS

SYNC DATE=01/11/2012

PAGE TITLE

CPU Constraints



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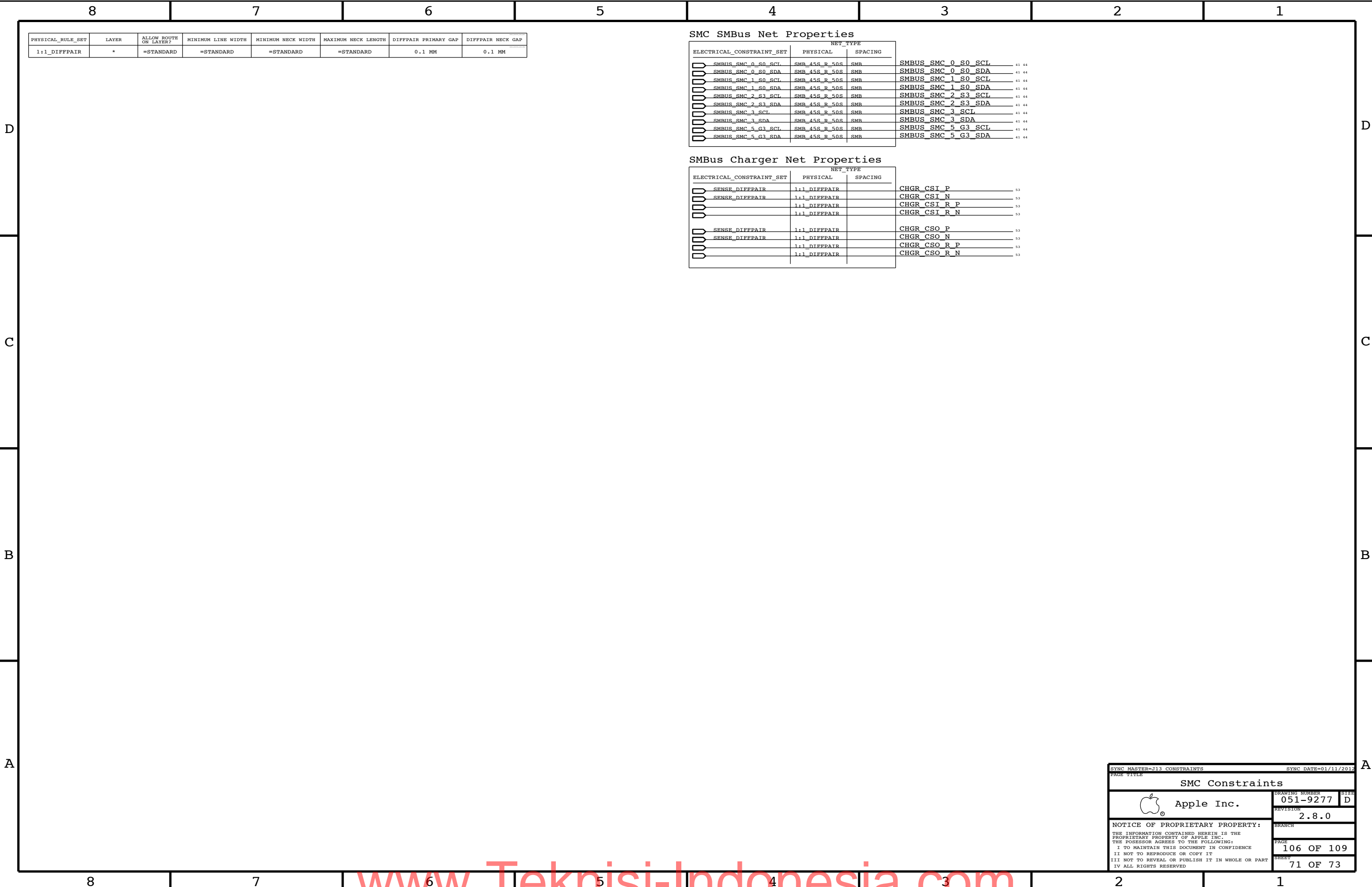
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<table><tr><td>PHYSICAL_RULE_SET</td><td>LAYER</td><td>ALLOW_ROUTE_ON_LAYER?</td><td>MINIMUM_LINE_WIDTH</td><td>MINIMUM_NECK_WIDTH</td><td>MAXIMUM_NECK_LENGTH</td><td>DIFFPAIR_PRIMARY_GAP</td><td>DIFFPAIR_NECK_GAP</td></tr><tr><td>SENSE_1TO1_45S</td><td>*</td><td>=1:1_DIFFPAIR</td><td>=45_OHM_SE</td><td>=45_OHM_SE</td><td>=45_OHM_SE</td><td>=1:1_DIFFPAIR</td><td>=1:1_DIFFPAIR</td></tr><tr><td>SENSE_1TO1_P2MM</td><td>*</td><td>=1:1_DIFFPAIR</td><td>0.200 MM</td><td>0.100 MM</td><td>=1:1_DIFFPAIR</td><td>=1:1_DIFFPAIR</td><td>=1:1_DIFFPAIR</td></tr><tr><td>THERM_1TO1_45S</td><td>*</td><td>=1:1_DIFFPAIR</td><td>=45_OHM_SE</td><td>=45_OHM_SE</td><td>=45_OHM_SE</td><td>=1:1_DIFFPAIR</td><td>=1:1_DIFFPAIR</td></tr><tr><td>SPKR_DIFFPAIR</td><td>*</td><td>=1:1_DIFFPAIR</td><td>0.300 MM</td><td>0.100 MM</td><td>=1:1_DIFFPAIR</td><td>=1:1_DIFFPAIR</td><td>=1:1_DIFFPAIR</td></tr></table>				PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM_LINE_WIDTH	MINIMUM_NECK_WIDTH	MAXIMUM_NECK_LENGTH	DIFFPAIR_PRIMARY_GAP	DIFFPAIR_NECK_GAP	SENSE_1TO1_45S	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR	SENSE_1TO1_P2MM	*	=1:1_DIFFPAIR	0.200 MM	0.100 MM	=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR	THERM_1TO1_45S	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR	SPKR_DIFFPAIR	*	=1:1_DIFFPAIR	0.300 MM	0.100 MM	=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR	<table><tr><td>SPACING_RULE_SET</td><td>LAYER</td><td>LINE-TO-LINE_SPACING</td><td>WEIGHT</td></tr><tr><td>SENSE</td><td>*</td><td>=2:1_SPACING</td><td>?</td></tr><tr><td>THERM</td><td>*</td><td>=2:1_SPACING</td><td>?</td></tr><tr><td>AUDIO</td><td>*</td><td>=2:1_SPACING</td><td>?</td></tr></table>				SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT	SENSE	*	=2:1_SPACING	?	THERM	*	=2:1_SPACING	?	AUDIO	*	=2:1_SPACING	?	<table><tr><td>NET_SPACING_TYPE1</td><td>NET_SPACING_TYPE2</td><td>AREA_TYPE</td><td>SPACING_RULE_SET</td></tr><tr><td>CPU_COMP</td><td>GND</td><td>*</td><td>GND_P2MM</td></tr><tr><td>CPU_VCCSENSE</td><td>GND</td><td>*</td><td>GND_P2MM</td></tr></table>				NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	CPU_COMP	GND	*	GND_P2MM	CPU_VCCSENSE	GND	*	GND_P2MM																																																																																																																																																																																																																																																																							
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CPU_VCCSENSE	GND	*	GND_P2MM																																																																																																																																																																																																																																																																																																																																																			
<table><tr><td>NET_SPACING_TYPE1</td><td>NET_SPACING_TYPE2</td><td>AREA_TYPE</td><td>SPACING_RULE_SET</td></tr><tr><td>GND</td><td>CLK_PCIE</td><td>*</td><td>GND_P2MM</td></tr><tr><td>GND</td><td>PCIE*</td><td>*</td><td>GND_P2MM</td></tr><tr><td>GND</td><td>SATA*</td><td>*</td><td>GND_P2MM</td></tr><tr><td>GND</td><td>USB*</td><td>*</td><td>GND_P2MM</td></tr><tr><td>GND</td><td>LVDS*</td><td>*</td><td>GND_P2MM</td></tr><tr><td>SB_POWER</td><td>CLK_PCIE</td><td>*</td><td>PWR_P2MM</td></tr><tr><td>SB_POWER</td><td>SATA*</td><td>*</td><td>PWR_P2MM</td></tr><tr><td>SB_POWER</td><td>SATA*</td><td>*</td><td>PWR_P2MM</td></tr></table>				NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	GND	CLK_PCIE	*	GND_P2MM	GND	PCIE*	*	GND_P2MM	GND	SATA*	*	GND_P2MM	GND	USB*	*	GND_P2MM	GND	LVDS*	*	GND_P2MM	SB_POWER	CLK_PCIE	*	PWR_P2MM	SB_POWER	SATA*	*	PWR_P2MM	SB_POWER	SATA*	*	PWR_P2MM																																																																																																																																																																																																																																																																																																															
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SB_POWER	SATA*	*	PWR_P2MM																																																																																																																																																																																																																																																																																																																																																			
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<table><tr><td>SPACING_RULE_SET</td><td>LAYER</td><td>LINE-TO-LINE_SPACING</td><td>WEIGHT</td></tr><tr><td>GND_P2MM</td><td>*</td><td>0.20 MM</td><td>1000</td></tr><tr><td>PWR_P2MM</td><td>*</td><td>0.20 MM</td><td>1000</td></tr></table>				SPACING_RULE_SET	LAYER	LINE-TO-LINE_SPACING	WEIGHT	GND_P2MM	*	0.20 MM	1000	PWR_P2MM	*	0.20 MM	1000																																																																																																																																																																																																																																																																																																																																							
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PWR_P2MM	*	0.20 MM	1000																																																																																																																																																																																																																																																																																																																																																			
<h3>J11/J13 Specific Net Properties</h3> <table><tr><th rowspan="2">ELECTRICAL_CONSTRAINT_SET</th><th colspan="2">NET_TYPE</th></tr><tr><th>PHYSICAL</th><th>SPACING</th></tr><tr><td> SENSE_DIFFPAIR</td><td>THERM_1TO1_45S</td><td>THERM</td><td>INLET_THMSNS_D1_P</td><td>46</td><td>47</td></tr><tr><td> SENSE_DIFFPAIR</td><td>THERM_1TO1_45S</td><td>THERM</td><td>INLET_THMSNS_D1_N</td><td>46</td><td>47</td></tr><tr><td> SENSE_DIFFPAIR</td><td>THERM_1TO1_45S</td><td>THERM</td><td>TBT_THERMD_P</td><td>47</td><td></td></tr><tr><td> SENSE_DIFFPAIR</td><td>THERM_1TO1_45S</td><td>THERM</td><td>TBT_THERMD_N</td><td>47</td><td></td></tr><tr><td> SENSE_DIFFPAIR</td><td>THERM_1TO1_45S</td><td>THERM</td><td>TBT_MLBBOT_THMSNS_P</td><td>47</td><td></td></tr><tr><td> SENSE_DIFFPAIR</td><td>THERM_1TO1_45S</td><td>THERM</td><td>TBT_MLBBOT_THMSNS_N</td><td>47</td><td></td></tr><tr><td> SENSE_DIFFPAIR</td><td>THERM_1TO1_45S</td><td>THERM</td><td>TBTTTHMSNS_D2_R_P</td><td>47</td><td></td></tr><tr><td> SENSE_DIFFPAIR</td><td>THERM_1TO1_45S</td><td>THERM</td><td>TBTTTHMSNS_D2_R_N</td><td>47</td><td></td></tr><tr><td> SENSE_DIFFPAIR</td><td>SENSE_1TO1_45S</td><td>SENSE</td><td>CPU_THERMD_P</td><td>9</td><td>47</td></tr><tr><td> SENSE_DIFFPAIR</td><td>SENSE_1TO1_45S</td><td>SENSE</td><td>CPU_THERMD_N</td><td>9</td><td>47</td></tr><tr><td> SENSE_DIFFPAIR</td><td>SENSE_1TO1_45S</td><td>SENSE</td><td>CPUTHMSNS_D2_P</td><td>47</td><td></td></tr><tr><td> SENSE_DIFFPAIR</td><td>SENSE_1TO1_45S</td><td>SENSE</td><td>CPUTHMSNS_D2_N</td><td>47</td><td></td></tr><tr><td> SENSE_DIFFPAIR</td><td>SENSE_1TO1_P2MM</td><td>SENSE</td><td>CPUVCCIOS0_CS_N</td><td>45</td><td>59</td></tr><tr><td> SENSE_DIFFPAIR</td><td>SENSE_1TO1_P2MM</td><td>SENSE</td><td>CPUVCCIOS0_CS_P</td><td>45</td><td>59</td></tr><tr><td> SENSE_DIFFPAIR</td><td>SENSE_1TO1_P2MM</td><td>SENSE</td><td>CPUIMVP_ISNS1_P</td><td>45</td><td>57</td></tr><tr><td> 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SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_N	8	46																																																																																																																																																																																																																																																																																																																																																	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_P	8	46																																																																																																																																																																																																																																																																																																																																																	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER_N	46																																																																																																																																																																																																																																																																																																																																																		
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SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V5_S3_N	46	56																																																																																																																																																																																																																																																																																																																																																	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V5_S3_P	46	56																																																																																																																																																																																																																																																																																																																																																	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_N	37	46																																																																																																																																																																																																																																																																																																																																																	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_P	37	46																																																																																																																																																																																																																																																																																																																																																	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_SSD_N	38	46																																																																																																																																																																																																																																																																																																																																																	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_SSD_P	38	46																																																																																																																																																																																																																																																																																																																																																	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_N	8	46																																																																																																																																																																																																																																																																																																																																																	
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_P	8	46																																																																																																																																																																																																																																																																																																																																																	
AUD_DIFF	1:1_DIFFPAIR	AUDIO	SPKRAMP_INR_P	6	40																																																																																																																																																																																																																																																																																																																																																	
AUD_DIFF	1:1_DIFFPAIR	AUDIO	SPKRAMP_INR_N	6	40																																																																																																																																																																																																																																																																																																																																																	
SENSE_DIFFPAIR	1:1_DIFFPAIR	AUDIO	MAX98300_R_P	51																																																																																																																																																																																																																																																																																																																																																		
SENSE_DIFFPAIR	1:1_DIFFPAIR	AUDIO	MAX98300_R_N	51																																																																																																																																																																																																																																																																																																																																																		
SENSE_DIFFPAIR	1:1_DIFFPAIR	AUDIO	SPKRAMP_ROUT_P	6	51																																																																																																																																																																																																																																																																																																																																																	
SENSE_DIFFPAIR	1:1_DIFFPAIR	AUDIO	SPKRAMP_ROUT_N	6	51																																																																																																																																																																																																																																																																																																																																																	
SB_POWER		SB_POWER	PP3V3_S5	6	7																																																																																																																																																																																																																																																																																																																																																	
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GND		GND	GND																																																																																																																																																																																																																																																																																																																																																			
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Project Specific Constraints

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## J11/J13 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM	NO_TYPE, BGA	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	TOP, BOTTOM	Y	=50_OHM_SE	=50_OHM_SE			
DEFAULT	ISL2, ISL11	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	ISL3, ISL10	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	ISL4, ISL9	Y	=45_OHM_SE	=45_OHM_SE			
DEFAULT	*	N	100 MM	100 MM	10 MM	0 MM	0 MM
STANDARD	*	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT

## Single-ended Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.310 MM			
27P4_OHM_SE	ISL2,ISL11	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	ISL3,ISL10	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	ISL4,ISL9	Y	0.182 MM	0.182 MM			
27P4_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_OHM_SE	TOP,BOTTOM	Y	0.195 MM	0.195 MM			
35_OHM_SE	ISL2,ISL11	Y	0.125 MM	0.125 MM			
35_OHM_SE	ISL3,ISL10	Y	0.125 MM	0.125 MM			
35_OHM_SE	ISL4,ISL9	Y	0.125 MM	0.125 MM			
35_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.170 MM	0.170 MM			
40_OHM_SE	ISL2,ISL11	Y	0.096 MM	0.096 MM			
40_OHM_SE	ISL3,ISL10	Y	0.096 MM	0.096 MM			
40_OHM_SE	ISL4,ISL9	Y	0.099 MM	0.099 MM			
40_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.135 MM	0.135 MM			
45_OHM_SE	ISL2,ISL11	Y	0.075 MM	0.075 MM			
45_OHM_SE	ISL3,ISL10	Y	0.075 MM	0.075 MM			
45_OHM_SE	ISL4,ISL9	Y	0.080 MM	0.080 MM			
45_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.110 MM			
50_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

## Differential Pair Physical Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	TOP,BOTTOM	Y	0.165 MM	0.165 MM		0.130 MM	0.130 MM
72_OHM_DIFF	ISL2,ISL11	Y	0.109 MM	0.109 MM		0.150 MM	0.150 MM
72_OHM_DIFF	ISL3,ISL10	Y	0.109 MM	0.109 MM		0.150 MM	0.150 MM
72_OHM_DIFF	ISL4,ISL9	Y	0.114 MM	0.114 MM		0.150 MM	0.150 MM
72_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	TOP,BOTTOM	Y	0.132 MM	0.132 MM		0.130 MM	0.130 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.081 MM	0.081 MM		0.115 MM	0.115 MM
80_OHM_DIFF	ISL3,ISL10	Y	0.081 MM	0.081 MM		0.115 MM	0.115 MM
80_OHM_DIFF	ISL4,ISL9	Y	0.088 MM	0.088 MM		0.110 MM	0.110 MM
80_OHM_DIFF	*	N	100 MM	100 MM	=STANDARD	=STANDARD	=STANDARD


## Spacing Constraints

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.100 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP,BOTTOM	0.071 MM	?
1x_DIELECTRIC	ISL3,ISL10	0.053 MM	?
1x_DIELECTRIC	ISL4,ISL9	0.050 MM	?
1x_DIELECTRIC	*	0.090 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM

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